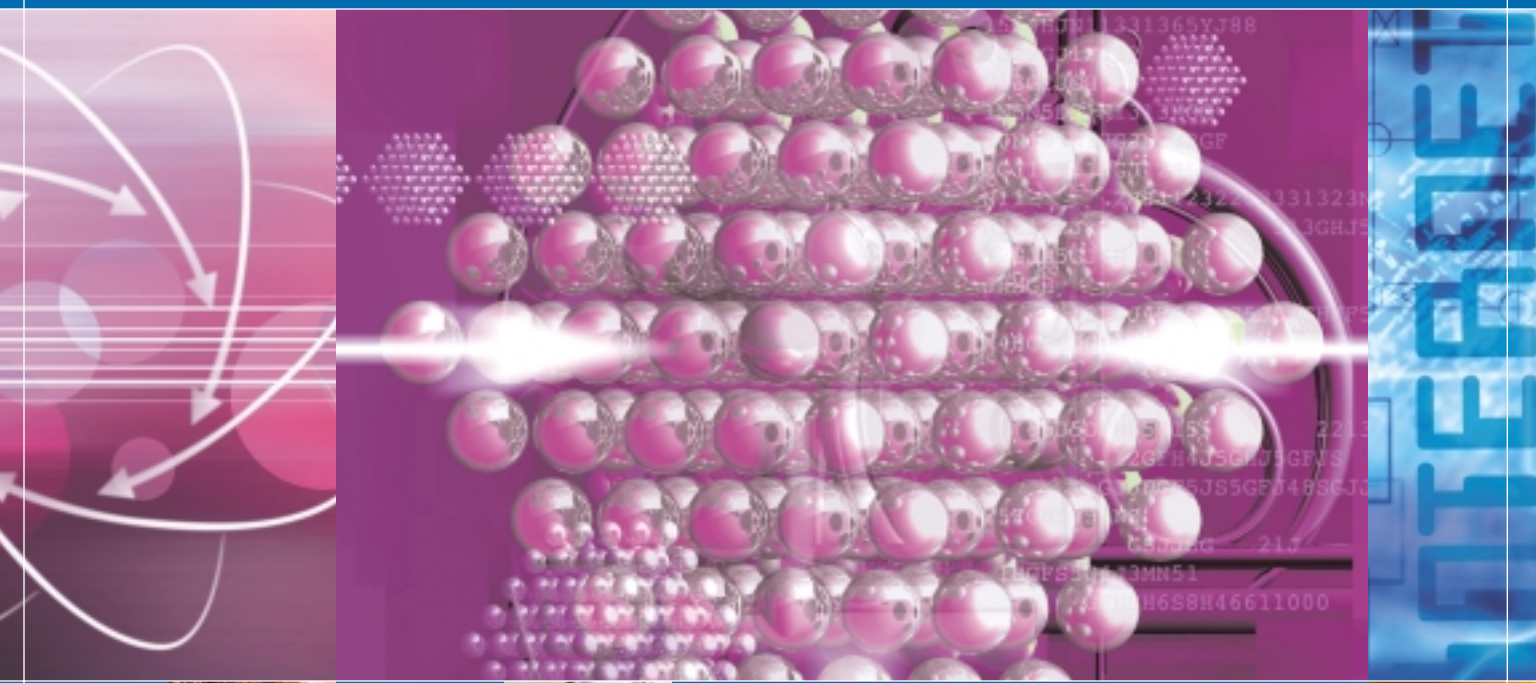
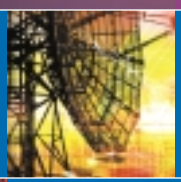
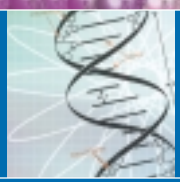
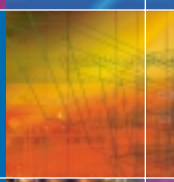
ADVANCE PROGRAM

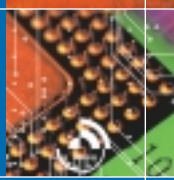
9th International Conference on High Performance Computing











December 18-21, 2002
Bangalore, India

www.hipc.org

ACKNOWLEDGMENTS

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Fax: +91-80-558-4520

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Taj Residency

Due to large number of activities on December 18, some tutorials will be held at an alternate location. Check the HiPC website for location information.

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Steve Olariu, Old Dominion University
Michael Palis, Rutgers University at Camden
Parmesh Ramanathan, University of Wisconsin, Madison
Ramesh Rao, University of California, San Diego
Krishna Sivalingam, Washington State University

SYSTEMS SOFTWARE
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Hamid Arabnia, University of Georgia
Jiannong Cao, Hong Kong Polytechnic University
Elizier Dekel, IBM Research Laboratory, Haifa
R. Govindarajan, Indian Institute of Science
Weijia Jia, City University of Hong Kong
Rajib Mall, Indian Institute of Technology, Kharagpur
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Cheng-zhong Xu, Wayne State University

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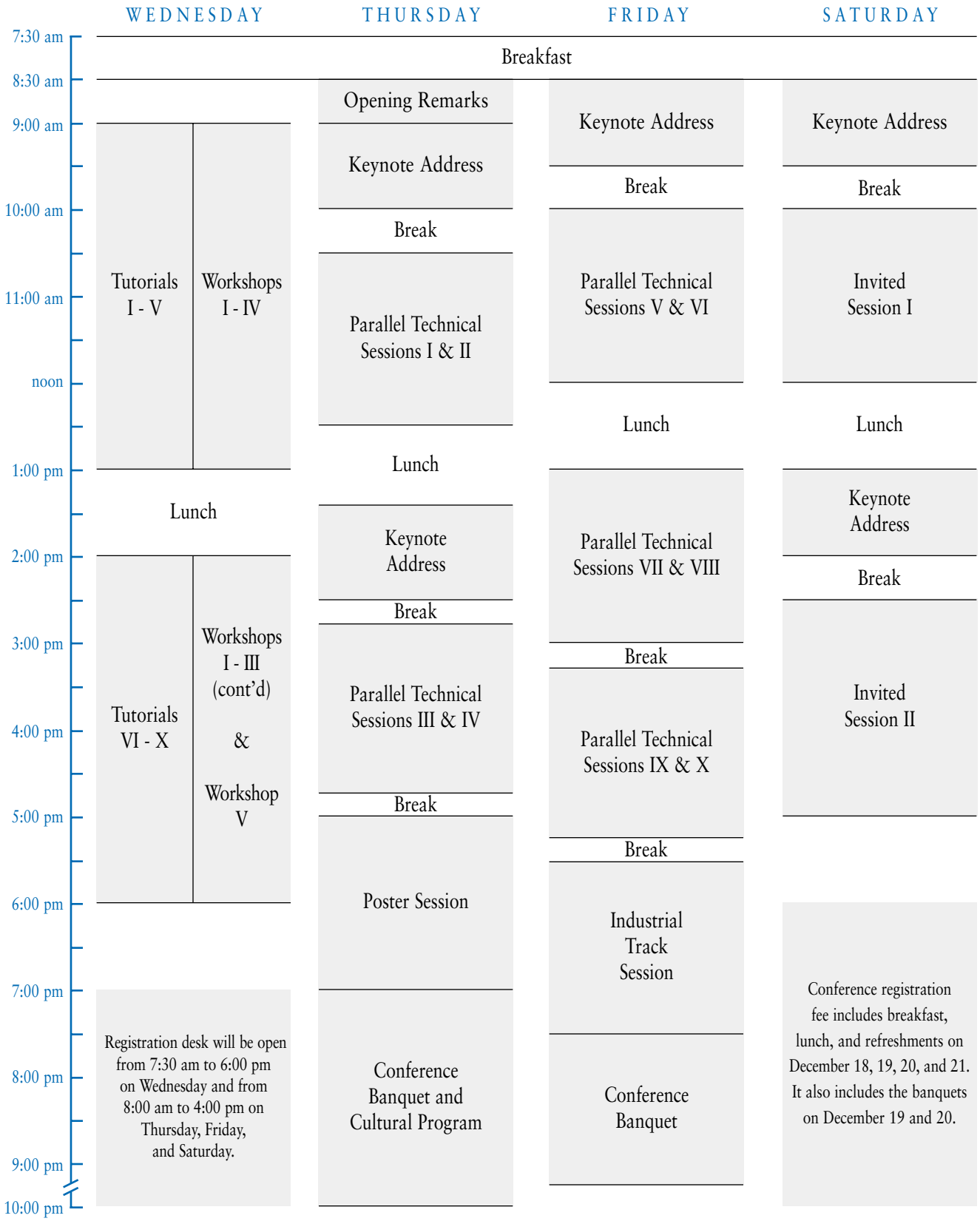
SCHEDULE


WEDNESDAY
THURSDAY
FRIDAY
SATURDAY
7:30 am
8:30 am
9:00 am
10:00 am
11:00 am
noon
1:00 pm
2:00 pm
3:00 pm
4:00 pm
5:00 pm
6:00 pm
7:00 pm
8:00 pm
9:00 pm
10:00 pm
Breakfast
Tutorials I - V
Workshops I - IV
Lunch
Tutorials VI - X
Workshops I - III (cont'd) & Workshop V
Registration desk will be open from 7:30 am to 6:00 pm on Wednesday and from 8:00 am to 4:00 pm on Thursday, Friday, and Saturday.
Opening Remarks
Keynote Address
Break
Parallel Technical Sessions I & II
Lunch
Keynote Address
Break
Parallel Technical Sessions III & IV
Break
Poster Session
Conference Banquet and Cultural Program
Keynote Address
Break
Parallel Technical Sessions V & VI
Lunch
Parallel Technical Sessions VII & VIII
Break
Parallel Technical Sessions IX & X
Break
Industrial Track Session
Conference Banquet
Keynote Address
Break
Invited Session I
Lunch
Keynote Address
Break
Invited Session II
Conference registration fee includes breakfast, lunch, and refreshments on December 18, 19, 20, and 21. It also includes the banquets on December 19 and 20.

OVERVIEW

KEYNOTE SPEAKERS

Imrich Chlamtac
University of Texas at Dallas
"Protocols for Bandwidth Management in Third Generation Optical Networks"

Patrick Lysaght
Xilinx Research Labs
"Beyond FPGAs, Field Programmable Systems"

B. Vincent McKoy
California Institute of Technology
"Parallel Computations of Electron-Molecule Collisions in Processing Plasmas"

N. Radhakrishnan
Computational and Information Sciences Directorate, Army Research Labs, USA
"Computational Science and Engineering -- Past, Present, and Future"

Priya Vashishta
University of Southern California
"Collaboratory for Info-Bio-Nano Simulations"

CONTRIBUTED PAPERS

There will be 57 contributed papers from 12 countries, chosen from 145 papers submitted in response to the call for papers. Contributed papers will be presented in 10 sessions.

INVITED PAPERS

Leading researchers will share their visions for biocomputation and embedded systems through invited papers to be presented in two plenary sessions.

Biocomputation
Organizer
Vijay Kumar
University of Pennsylvania

Embedded Systems
Organizer
Viktor K. Prasanna
University of Southern California

WORKSHOPS

Workshop on Bioinformatics and Computational Biology

Workshop on Soft Computing

Trusted Internet Workshop

Workshop on Cutting Edge Computing

Workshop on Storage Area Networks

POSTER/PRESENTATION SESSION

A plenary poster/presentation session emphasizing novel applications of high performance computing will be held on Thursday, 19 December. It will offer a brief presentation time for each poster followed by a walk-up and talk setting.

For details, contact:
Paul Roe
Queensland University of Technology
Email: p.roe@qut.edu.au

Rajkumar Buyya
The University of Melbourne
Email: rajkumar@buyya.com

TUTORIALS

Computational Methods in Bioinformatics
Sharmila S. Mande and M. Vidyasagar
Tata Consultancy Services

Writing Parallel Programs with OpenMP
Timothy G. Mattson
Intel Corporation

Data Stream Mining in Mobile and Distributed Environments
Hillol Kargupta
University of Maryland Baltimore County

The Early 21st Century Processor Architecture Landscape
Sriram Vajapeyam
Independent Consultant

Wireless Sensor Network Protocols
Krishna M. Sivalingam
Washington State University

Wireless Networking using IEEE 802.11 and Bluetooth: Technology and Research Challenges
Pravin Bhagwat
Indian Institute of Technology, Kanpur and Winlab, Rutgers University
Rajeev Shorey
IBM India Research Laboratory and Indian Institute of Technology, New Delhi

Quantum Computing
Rajendra K. Bera
IBM Global Services India Pvt. Limited

Design for High Reliability, Availability and Serviceability
Dhiraj K. Pradhan
University of Bristol

Data Grid Management Systems: Towards Knowledge Grid Networks
Arcot Rajasekar and Arun Jagatheesan
San Diego Supercomputer Center
University of California, San Diego

Opportunities and Challenges in Pervasive Computing
Raju Pandey
University of California, Davis

THURSDAY, DEC. 19

KEYNOTES & TECHNICAL SESSIONS

8:30 am - 9:00 am

INAUGURATION

by
V. Kulakarni, IAS
Department of Information
Technology & Biotechnology
Govt. of Karnataka

Guest of Honor
S. Sadagopan
Indian Institute of Information
Technology, Bangalore

OPENING REMARKS

Viktor K. Prasanna
Uday Shukla
Sartaj Sahni

9:00 am - 10:00 am

KEYNOTE ADDRESS

"Collaboratory for Info-Bio-Nano Simulations"
Priya Vashishta
University of Southern California

Priya Vashishta is the Director of High Performance Computing Center at the University of Southern California. He is a professor in the Departments of Materials Science & Engineering and Computer Science, and Physics and Biomedical Engineering. Prior to joining USC, during 1990-2002, he was Cray Research Professor of Computational Sciences and the founding director of the Concurrent Computing Laboratory for Materials Simulations at the Louisiana State University. From 1972-1990, he was at the Argonne National Laboratory as a Senior Scientist and the Director of the Solid State Sciences Division.

His research includes developing multiscale simulation approach that combines electronic structure, molecular dynamics, and finite-element methods. Visualization tools are also being designed to analyze simulations in immersive and interactive virtual environments. These large-scale multimillion atom simulations have been executed with highly efficient, portable and scalable, multi-resolution algorithms.

10:30 am - 12:30 pm

SESSION I

Algorithms I
Chair: Bhabani Sinha
Indian Statistical Institute

2-D Wavelet Transform Enhancement on General-Purpose Microprocessors: Memory Hierarchy and SIMD Parallelism Exploitation
D. Chaver, C. Tenllado, L. Piñuel, M. Prieto, and F. Tirado, Universidad Complutense

A General Data Layout for Distributed Consistency in Data Parallel Applications
Roxana Diaconescu, Norwegian University of Science and Technology

A Parallel DFA Minimization Algorithm
Ambuj Tewari, Utkarsh Srivastava, and P. Gupta, Indian Institute of Technology, Kanpur

Accelerating the CKY Parsing using FPGAs
Jacir L. Bordim, Yasuaki Ito, and Koji Nakano, Japan Advanced Institute of Science and Technology

Duplication based Scheduling Algorithm for Interconnection Constrained Distributed Memory Machines
Savina Bansal, Padam Kumar, and Kuldip Singh, Indian Institute of Technology, Roorkee

Evaluating Arithmetic Expressions using Tree Contraction: A Fast and Scalable Parallel Implementation for Symmetric Multiprocessors (SMPS)
David A. Bader, Sukanya Sreshta, and Nina R. Weisse-Bernstein, University of New Mexico

10:30 am - 12:30 pm

SESSION II

Architecture I
Chair: Michel Cosnard
INRIA, France

Dead-block Elimination in Cache: A Mechanism to Reduce I-Cache Power Consumption in High Performance Microprocessors
Mohan G. Kabadi, Natarajan Kannan, Palanidaran Chidambaram, Suriya Narayanan, M. Subramanian, and Ranjani Parthasarathi, Anna University

Exploiting Web Document Structure to Improve Storage Management in Proxy Caches
Abdolreza Abhari, Sivarama Dandamudi, and Shikharesh Majumdar, Carleton University

High Performance Multiprocessor Architecture Design Methodology for Application-Specific Embedded Systems
Syed Saif Abrar, Phillips Semiconductors, Bangalore

LLM: A Low Latency Messaging Infrastructure for Linux Clusters
R. K. Shyamasundar, Basant Rajan, Manish Prasad, and Amit Jain, Tata Institute of Fundamental Research

Low-Power High-Performance Adaptive Computing Architectures for Multimedia Processing
Rama Sangireddy and Arun K. Somani, Iowa State University

THURSDAY, DEC. 19

KEYNOTES & TECHNICAL SESSIONS

1:30 pm - 2:30 pm

KEYNOTE ADDRESS

"Beyond FPGAs, Field Programmable Systems"
Patrick Lysaght
Xilinx Research Labs

Patrick Lysaght is a Senior Director in Xilinx Research Labs where he leads research into emerging design technologies. Previously, he worked in research, development, marketing, technical support, sales and education in Scotland, for such organizations as the Institute for Systems Level Integration, the University of Strathclyde and Hewlett Packard. Patrick holds BSc and MSc degrees in electronics. He has published forty technical papers relating to dynamically reconfigurable logic. He is a chairman of the steering committee for FPL, the world's largest field programmable logic conference.

2:45 pm - 4:45 pm

SESSION III

Systems Software I
Chair: Rajib Mall
Indian Institute of Technology, Kharagpur

CORBA-as-Needed: A Technique to Construct High Performance CORBA Applications
Hui Dai, Shivakant Mishra, University of Colorado and Matti A. Hiltunen, AT&T Research Labs

Automatic Search for Performance Problems in Parallel and Distributed Programs by using Multi-Experiment Analysis
Thomas Fahringer and Clovis Seragiotto Jr., University of Vienna

An Adaptive Value-based Scheduler and its RT-Linux Implementation
S. Swaminathan and G. Manimaran, Iowa State University

Effective Selection of Partition Sizes for Moldable Scheduling of Parallel Jobs
Srividya Srinivasan, Vijay Subramani, Rajkumar Kettimuthu, Praveen Holenarsipur, and P. Sadayappan, Ohio State University

Runtime Support for Multigrain and Multiparadigm Parallelism
Panagiotis E. Hadjidoukas, Eleftherios D. Polychronopoulos, and Theodore S. Papatheodorou, University of Patras

A Fully Compliant OpenMP Implementation on Software Distributed Shared Memory
Sung-Woo Lee, Sven Karlsson, and Mats Brorsson, Royal Institute of Technology

2:45 pm - 4:45 pm

SESSION IV

Networks
Chair: Abhay Karandikar
Indian Institute of Technology, Mumbai

A Fast Connection-Time Redirection Mechanism for Internet Application Scalability
Michael Haungs, Raju Pandey, Earl Barr, University of California, Davis, and J. Fritz Barnes, Vanderbilt University

Algorithms for Switch-Scheduling in the Multimedia Router for LANs
Indrani Paul, Sudhakar Yalamanchili, Georgia Institute of Technology, and Jose Duato, Universite Politecnia de Valencia

An Efficient Resource Sharing Scheme for Dependable Real-Time Communication in Multihop Networks
G. Ranjith and C. Siva Ram Murthy, Indian Institute of Technology, Chennai

Improving Web Server Performance by Network Aware Data Buffering and Caching
Sourav Sen and Y. Narahari, Indian Institute of Science

Wraps Scheduling and its Efficient Implementation on Network Processors
Xiaotong Zhuang and Jian Liu, Georgia Institute of Technology

Performance Comparison of Pipelined Hash Joins on Workstation Clusters
Kenji Imasaki, Hong Nguyen, and Sivarama P. Dandamudi, Carleton University

5:00 pm - 7:00 pm

POSTER/PRESENTATION SESSION

This session will emphasize novel applications of high performance computing. It will offer a brief presentation time for each poster followed by a walk-up and talk setting. For submission details, contact:

Co-Chairs:
Paul Roe
Email: p.roe@qut.edu.au

Rajkumar Buyya
Email: rajkumar@buyya.com

7:00 pm - 10:00 pm

CONFERENCE BANQUET AND CULTURAL PROGRAM

FRIDAY, DEC. 20

KEYNOTES & TECHNICAL SESSIONS

8:30 am - 9:30 am

KEYNOTE ADDRESS

"Computational Science and Engineering – Past, Present, and Future"

N. Radhakrishnan
Computational and Information Sciences Directorate, Army Research Labs, USA

Dr. N. Radhakrishnan joined the Army Research Laboratory (ARL) in June 1999 as a Senior Executive Service (SES) member, as the Director of Computational and Information Sciences Directorate. The Directorate does research in Battlefield Communications, Data Fusion and Knowledge Management, Computational Science and Engineering, and Battlespace Environment and Atmospheric Science. Dr. Radha is also responsible for running a DOD High Performance Computing Center specializing in state-of-the-art scalable and vector computing hardware, scientific visualization, etc., and collaboration with researchers and academia in a number of application areas such as CFD, CSM, and CCM. He also funds the Army High Performance Computing Research Center (AHPCRC) currently located at the University of Minnesota. Dr. Radha is also the Chief Information Officer (CIO) for ARL and in this capacity is responsible for providing the Information Technology infrastructure for ARL.

Prior to taking the current position with ARL, Dr. Radha was the first Director of the Information Technology Laboratory (ITL) at the U.S. Army Corps of Engineers Waterways Experiment Station (WES). He was responsible for running one of the DoD High Performance Computing Centers, the Corps of Engineers Regional Processing Center, the DOD Tri-Services CADD/GIS Technology Center, the Corps of Engineers Software Engineering Center, and the Design Guidance Update Center.

Dr. Radha earned his bachelor's degree in engineering from Madras University, Madras, India, and his master's in engineering from the Indian Institute of Technology in Bombay. He earned his doctorate in engineering from the University of Texas at Austin.

10:00 am - noon

SESSION V

Algorithms II

Chair: Rajendra Bera
IBM Global Services India Pvt. Limited

Iterative Algorithms on Heterogeneous Network Computing: Parallel Polynomial Root Extracting
Raphael Couturier, Philippe Canalda, and Francois Spies, The University Franche-Comte

Optimal Tree-based Multicast in Wormhole-Routed Networks
Jianping Song, Zifeng Hou, and Yadong Qu, Wireless Communication Technology Lab, Beijing

Parallel Algorithms for Identification of Basis Polygons in an Image
Arijit Laha, National Institute of Management and Bhabani P. Sinha, Indian Statistical Institute

Range Image Segmentation on a Cluster
M. E. Bock, Purdue University and C. Guerra, Padova University and Purdue University

Detection of Orthogonal Interval Relations
Punit Chandra and Ajay Kshemkalyani, University of Illinois at Chicago

An Efficient Parallel Algorithm for Computing Bicompatible Elimination Ordering (BCO) of Proper Interval Graphs
B. S. Panda, University of Hyderabad and Sajal K. Das, University of Texas at Arlington

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SESSION VI

Mobile Computing and Databases

Chair: Nalini Venkatasubramanian
University of California, Irvine

Router Handoff: An Approach for Preemptive Route Repair in Mobile Adhoc Networks
Abhilash P., Srinath Perur, and Sridhar Iyer, Indian Institute of Technology, Bombay

A Two-Dimensional Random Walk based Mobility Model for Location Tracking
S. Mukhopadhyaya and K. Mukhopadhyaya, Indian Statistical Institute

Data Placement in Intermittently Available Environments
Yun Huang and Nalini Venkatasubramanian, University of California, Irvine

RT-MUPAC: Multi-Power Architecture for Voice Cellular Networks
K. Jayanth Kumar, B. S. Manoj, and C. Siva Ram Murthy, Indian Institute of Technology, Chennai

Asynchronous Transaction Processing for Updates by Client: With Elimination of Wait-for State
Subhash Bhalla, University of Aizu

Active File Systems for Data Mining and Multimedia
S H Srinivasan and Pranay Singh, Satyam Computer Services

FRIDAY, DEC. 20

KEYNOTES & TECHNICAL SESSIONS

1:00 pm - 3:00 pm

SESSION VII

Applications
Chair: Shahrouz Aliabadi
Clark Atlanta University

Simulating DNA Computing
Sanjeev Baskiyar, Auburn University

Parallel Syntenic Alignments
Natsuhiko Futamura, Srinivas Aluru, and Xiaoqiu Huang, Iowa State University

XS-Systems: Extended S-Systems and Algebraic Differential Automata for Modeling Cellular Behavior
Marco Antoniotti, Courant, New York University, Alberto Policriti, Universita` di Udine, Nadia Ugel, Courant, New York University, and Bud Mishra, Courant, New York University and Watson School

A High Performance Scheme for EEG Compression using a Multichannel Model
D. Gopikrishna and A. Makur, Indian Institute of Science

Scalability and Performance of Multi-Threaded Algorithms for International Fare Construction on High-Performance Machines
Krishnan Saranathan, Chandra N. Sekharan, Raj Sivakumar, United Airlines, and Zia Taherbhai, Loyola University of Chicago

1:00 pm - 3:00 pm

SESSION VIII

Systems Software II
Chair: P. Sadayappan
Ohio State University

A Resource Brokerage Infrastructure for Computational Grids
Ahmed Al-Theneyan, Old Dominion University, Piyush Mehrotra, NASA Ames Research Center, and Mohammad Zubair, Old Dominion University

On Improving Thread Migration: Safety and Performance
Hai Jiang and Vipin Chaudhary, Wayne State University

Improved Preprocessing Methods for Modulo Scheduling Algorithms
D. V. Ravindra and Y. N. Srikant, Indian Institute of Science

Dynamic Path Profile Aided Recompilation in a Java Just-in-Time Compiler
R. Vinodh Kumar, Cisco Systems, Bangalore, B. Lakshmi Narayanan, Anna University, Chennai, and R. Govindarajan, Indian Institute of Science

Exploiting Data Value Prediction in Compiler Based Thread Formation
Anasua Bhowmik and Manoj Franklin, University of Maryland

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SESSION IX

Scientific Computation
Chair: R. K. Shyamasundar
Tata Institute of Fundamental Research

High Performance Computing of Fluid-Structure Interactions in Hydrodynamics Applications using Unstructured Meshes with more than one Billion Elements
S. Aliabadi, A. Johnson, J. Abedi, and B. Zellars, Clark Atlanta University

Parallel Computers in Solving Elliptic Problems on Non-Smooth Domains by Spectral Element Methods
P. Dutt and B.V. Rathish Kumar, Indian Institute of Technology, Kanpur

Fast Stable Solver for Sequentially Semi-Separable Linear Systems of Equations
S. Chandrasekaran, P. Dewilde, M. Gu, T. Pals, and A. J. van der Veen, University of California, Santa Barbara

Dynamic Network Information Collection for Distributed Scientific Application Adaptation
Devdatta Kulkarni and Masha Sosonkina, University of Minnesota, Duluth

Adaptive Runtime Management of SAMR Applications
Sumir Chandra, Shweta Sinha, Manish Parashar, Rutgers University, Yeliang Zhang, Jingmei Yang, and Salim Hariri, University of Arizona

Mobile Agents - The Right Vehicle for Distributed Sequential Computing
Lei Pan, Lubomir F. Bic, and Michael B. Dillencourt, University of California, Irvine

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SESSION X

Architecture II
Chair: Siva Ram Murthy
Indian Institute of Technology, Chennai

Using Dataflow based Context for Accurate Branch Prediction
Renju Thomas and Manoj Franklin, University of Maryland

Rehashable BTB: An Adaptive Branch Target Buffer to Improve the Target Predictability of Java Code
Tao Li, Ravi Bhargava, and Lizy Kurian John, University of Texas, Austin

Return-Address Prediction in Speculative Multithreaded Environments
Mohamed Zahran and Manoj Franklin, University of Maryland

HLSPOWER: Hybrid Statistical Modeling of the Superscalar Power-Performance Design Space
Ravishankar Rao, University of California, Davis, Mark H. Oskin, University of Washington , and Frederic T. Chong, University of California, Davis

Efficient Decomposition Techniques for FPGAs
Seok-Bum Ko and Jien-Chung, University of Rhode Island

5:30 pm - 7:30 pm

INDUSTRIAL TRACK SESSION

(TBD)

7:30 pm - 9:30 pm

CONFERENCE BANQUET

BANQUET SPEECH

"Research in France in Computer Science and HPC"
Michel Cosnard
Université de Nice and
INRIA Sophia Antipolis, France

SATURDAY, DEC. 21

KEYNOTES & TECHNICAL SESSIONS

8:30 am - 9:30 am

KEYNOTE ADDRESS

"Protocols for Bandwidth Management in Third Generation Optical Networks"

Imrich Chlamtac
University of Texas at Dallas

Imrich Chlamtac is the Distinguished Chair in Telecommunications at the University of Texas at Dallas. Dr. Chlamtac also holds the titles of the Sackler Professor at Tel Aviv University, Israel and The Bruno Kessler Honorary Professor at the University of Trento, Italy and University Professorship, Hungary. He is a Fellow of the IEEE and ACM societies, the winner of the 2001 ACM Sigmobile and the IEEE ComSoc TCPC 2002 annual awards and recipient of multiple best paper awards and was Fulbright Scholar and IEEE Distinguished Lecturer. Dr. Chlamtac published close to three hundred articles on networking, and is the co-author of Local Area Networks, and Mobile and Wireless Networks Protocols and Services (John Wiley & Sons). Dr. Chlamtac serves as the Editor in Chief of the ACM/URSI/Kluwer Wireless Networks (WINET), and MONET journals and the SPIE/Kluwer Optical Networks (ONM) Magazine.

10:00 am - noon

INVITED SESSION I

Embedded Systems

Chair: Viktor K. Prasanna
University of Southern California

Memory Architecture Exploration for Embedded Systems
Nikil Dutt, University of California, Irvine

Structured Composition Techniques for Embedded Systems
Rajesh K. Gupta, University of California, San Diego

Low Power Distributed Embedded Systems: Dynamic Voltage Scaling and Synthesis
Jiong Luo and Niraj K. Jha, Princeton University

The Customization Landscape for Embedded Systems
Sudhakar Yalamanchili, Proceler Inc. and Georgia Institute of Technology

1:00 pm - 2:00 pm

KEYNOTE ADDRESS

"Parallel Computations of Electron-Molecule Collisions in Processing Plasmas"

B. Vincent Mckoy
California Institute of Technology

Vincent McKoy is Professor of Theoretical Chemistry at the California Institute of Technology where he has been a member of the faculty since 1964. He obtained his Ph.D. in Chemistry from Yale University in 1964. His research interests include theoretical and computational methods for studies of collisions of low-energy electrons in gases. A key feature of this effort has been the development of highly scalable strategies and algorithms which make it possible to exploit large parallel systems in such studies. These advances have enabled extensive applications to gases of interest in low-temperature plasmas that are widely used in the semiconductor industry.

He is a Fellow of the American Physical Society and is listed in Who's Who in America and in American Men of Science. He has been a Fellow of the Alfred P. Sloan and Guggenheim Memorial Foundations and received the Governor-General's (of Canada) Medal for Academic Excellence (1960).

2:30 pm - 5:00 pm

INVITED SESSION II

Biocomputation

Chair: Vijay Kumar
University of Pennsylvania

Computing Challenges in Systems Biology
Srikantha Kumar, Defense Advanced Research Projects Agency, USA

Visual Programming for Modeling and Simulation of Regulatory Networks
Rajeev Alur, Calin Belta, Franjo Ivancic, Vijay Kumar, Harvey Rubin, Jonathan Schug, and Oleg Sokolsky, University of Pennsylvania and Jonathan Webb, BBN

Framework for Open Source Software Development for Organ Simulation in the Digital Human
M. Cenk Cavusoglu, Tolga Goktekin, S. Shankar Sastry, University of California, Berkeley and Frank Tendick, University of California, San Francisco

Reachability Analysis of Delta-Notch Lateral Inhibition Using Predicate Abstraction
Inseok Hwang, Hamsa Balakrishnan, Ronojoy Ghosh and Claire Tomlin, Stanford University

A Symbolic Approach to Modeling Cellular Behavior
Bhubaneswar Mishra, Courant Institute, New York University

WEDNESDAY, DEC. 18

WORKSHOPS & TUTORIALS

9:00 am - 6:00 pm

WORKSHOP I

Workshop on Bioinformatics and Computational Biology

Discovery of biomolecular sequences and their relation to the functioning of organisms have created a number of challenging problems for computer scientists, and led to the emerging interdisciplinary field of bioinformatics and computational biology. The field holds immense potential for aiding in future discoveries such as the design of proteins for efficient administering of drugs and personalized medicine.

The goal of this workshop is to provide a forum for researchers and practitioners to discuss recent research and developments in bioinformatics and computational biology. The workshop will include contributed papers and invited talks.

Topics of interest include but are not limited to:
- Bioinformatic Databases
- Computational Genomics
- Computational Proteomics
- DNA Assembly, Clustering, and Mapping
- Gene Expression and Microarrays
- Gene Identification and Annotation
- Molecular Evolution
- Molecular Sequence Analysis
- Protein Structure

For further information contact the organizers.

Important Dates
September 30, 2002:
Workshop papers due

October 31, 2002:
Author notification

November 29, 2002:
Final papers due

ORGANIZERS
Srinivas Aluru
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For more information visit
http://vulcan.ee.iastate.edu/~aluru/bcb2002/

9:00 am - 6:00 pm

WORKSHOP II

Workshop on Soft Computing

Soft computing is a collection of techniques, whose goal is to exploit tolerance for imprecision, uncertainty and partial truth to achieve tractability, robustness and low solution cost. The Soft Computing term has been coined to include topics from Fuzzy Logic, Neural Networks and Genetic Algorithms. This field of Soft Computing is seeing a flurry of activity with a plethora of successful applications.

There have been several conferences organized, journals/magazines dedicated to this field. In the last few years, several successful commercial/industrial/defense/finance applications of soft computing techniques have emerged. The Workshop on Soft Computing is a step towards sharing the research results and new directions in the application and convergence of the areas of Fuzzy Logic, Neural Networks, Evolutionary Computing and Rough Sets. We intend to provide a platform for Soft Computing researchers for discussion and presentation of their work. In addition to paper presentations, we plan to have an industry-academia inter-action, poster sessions, tutorials on Soft Computing topics and exhibitions of soft computing products by industry.

There will be invited talks by leading researchers in the field.

Topics of interest include but are not limited to theory/applications of:
- Fuzzy Logic and Fuzzy Systems
- Neural Networks
- Neuro-Fuzzy Systems
- Genetic Algorithm

For further information contact the organizers.

Important Dates
October 02, 2002:
Workshop papers due
November 01, 2002:
Author notification
November 30, 2002:
Final papers due

ORGANIZER
Suthikshn Kumar
Larsen and Toubro Infotech Limited
Email: suthikshn.kumar@lntinfotech.com

For more information visit
http://wosco0.tripod.com/cfp1.html

9:00 am - 6:00 pm

WORKSHOP III

Trusted Internet Workshop

In recent years, there has been a tremendous push from business and user communities for next generation applications demanding Quality of Service (QoS), reliability, and security guarantees. The goal of Trusted Internet workshop is to provide a forum for researchers and practitioners to present and discuss their work and exchange ideas in the areas of Internet QoS, Internet Reliability, and Internet Security. To achieve this goal, this workshop solicits original, previously unpublished research contributions on (but not restricted to) the following subject categories of Trusted Internet:

- MPLS Networks
- DiffServ Networks
- Virtual Private Networks
- Content Distribution, Media Servers
- QoS Scheduling, Routing, Multicasting
- IP over WDM
- Optical Protection/Restoration
- Domain Name Server (DNS) Protection
- Denial of Service (DoS)
- Secure Internet Protocols
- WORMS
- Prototype Implementations and Studies
- Deployment Issues and Analysis

For further information contact the organizers.

Important Dates
October 01, 2002:
Workshop papers due
November 01, 2002:
Author notification
November 30, 2002:
Final papers due

ORGANIZERS
G. Manimaran
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For more information visit
http://vulcan.ee.iastate.edu/~gmani/tiw/

WEDNESDAY, DEC. 18

WORKSHOPS & TUTORIALS

9:00 am - 1:00 pm

WORKSHOP IV
Workshop on Cutting Edge Computing

This workshop will feature invited presentations from experts in such areas as Quantum Computing, Supercomputing/Deep Computing, Datamining of Scientific Data, etc. The goal is to bring to the attention of researchers and practitioners, recent R&D advances in computing technologies that are expected to dominate the future of computing.

Topics of interest include but are not limited to:
- Supercomputing/Deep Computing
  Grid Computing
- Quantum Computing
- Advanced Algorithms
- Datamining of Scientific Data
- Compiler Optimization

For further information contact the organizers.

ORGANIZERS
Uday S. Shukla
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Rajendra K. Bera
IBM Global Services India Pvt. Limited
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For more information visit
http://www.hipc.org/hipc2002/

2:00 pm - 6:00 pm

WORKSHOP V
Workshop on Storage Area Networks

In conventional computing systems, servers and storage devices inhabit the same box and communicate through a local bus. In Storage Area Networks (SAN) servers and storage deices can be geographically separate and the interconnection is through a high-speed network. SANs offer several advantages such as server-free backups, ease of management, resource sharing, etc. The goal of the workshop is to bring beginners, practitioners, and researchers together and to provide a glimpse of research, implementation, and deployment issues.

Topics of interest include but are not limited to:
- SAN Architectures
- SAN Management
- Storage Virtualization
- Security
- Storage over FC, IP, and Ethernet
- Standards

For further information contact the organizers.

Important Dates
October 04, 2002:
Workshop papers due
November 01, 2002:
Author notification
November 29, 2002:
Final papers due

ORGANIZERS
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For more information visit
http://satyamus.satyam.com/members/hipc/hipcworkshop.htm

9:00 am - 1:00 pm

TUTORIAL I
Computational Methods in Bioinformatics
Sharmila S. Mande and M. Vidyasagar
Tata Consultancy Services

Audience: The tutorial is intended as a introduction to Bioinformatics to students and professionals with an IT background.

Course Description: Technological advances in life sciences have been generating an immense amount of data. Computational methods have been applied to decipher useful information contained therein. The synergy between computer science and life science thus has led to the birth of Bioinformatics. In this tutorial, we will cover the following topics: 1) Basic molecular biology – Cellular organization, structure of the cell, chromosomes, genes, DNA, RNA, proteins, DNA Replication, transcription, translation, challenges in biology, 2) Sequence analysis – Local and global similarity searches, pairwise and multiple sequence alignments, 3) Genome annotation and analysis – ORF prediction algorithms for prokaryotes and eukaryotes, pattern identification, RNA structure prediction, 4) Protein structure – Primary, secondary, tertiary and quaternary structures, domains and motifs, secondary structure prediction methods, transmembrane prediction, various 3D modelling methods, and 5) Comparative genome analysis – Whole genome alignment, gene function identification.

Lecturers: Dr. Sharmila Mande heads the Bioinformatics Division at the Advanced Technology Centre of TCS. Her research interests are in comparative genomics, protein structure and protein-protein interactions She received her Ph. D. from Indian Institute of Science, Bangalore in 1991.

Dr. M. Vidyasagar is an Executive Vice President of TCS and heads the Advanced Technology Center in Hyderabad. His current research interests are statistical learning theory and the application of machine learning approaches to various problems in computational Biology. He received his Ph. D. from University of Wisconsin, Madison in 1969. He is the author of nine books and 130 journal articles, and has received several awards in recognition of his research.

9:00 am - 1:00 pm

TUTORIAL II

Writing Parallel Programs with OpenMP

Timothy G. Mattson
Intel Corporation

Audience: This course will be of value to programmers (C, C++ or Fortran) interested in learning about OpenMP. Experience with parallel programming is not required.

Course Description: The OpenMP Application Programming Interface (API) defines compiler directives and library routines that make it relatively easy to create programs for shared memory computers. It first appeared in 1997 and has become the de facto standard for programming shared memory computers. In this tutorial, we will provide a comprehensive overview of OpenMP. The OpenMP specifications are simple enough that in half a day we will be able to cover the entire API. We will start with basic concepts in programming shared memory computers and then move onto the basic constructs in OpenMP. This will include thread creation, assigning work to threads, managing data within the program and finally synchronization of threads. The focus of the tutorial is using OpenMP to write real applications. Therefore, we will demonstrate the OpenMP constructs using excerpts from real applications. We will use these applications to explain how to use the basic OpenMP constructs, but also how to use them effectively to maximize performance and robustness.

Lecturer: Dr. Mattson joined Intel in 1993 to work on a wide range of parallel computing issues. He was a senior scientist on the ASCI Teraflop computer project. Later, he helped write the OpenMP API for shared memory programming. He continues to play a key role with OpenMP and is currently serving as the CEO of the OpenMP Architecture Review Board. His most recent projects focus on parallel and distributed computing. He helped found the Open Cluster Group: an industry/national-laboratory collaboration dedicated to making clusters more appropriate for mainstream technical computing. The first project from this group is OSCAR: a robust and easy to use software stack for cluster computing. Prior to joining Intel, Dr. Mattson held a number of industrial and academic positions with a focus on scientific computing on high performance computers. He holds a Ph.D. (U.C. Santa Cruz, 1985) for his work on quantum scattering theory.

9:00 am - 1:00 pm

TUTORIAL III

Data Stream Mining in Mobile and Distributed Environments

Hillol Kargupta
University of Maryland Baltimore County

Audience: This tutorial will introduce attendees to issues involved in mobile and distributed data stream mining. It will assume that the audience has introductory knowledge of data mining, but no knowledge of data stream mining in a ubiquitous environment.

Course Description: This tutorial will present an overview of the state-of-the-art technology for ubiquitous data-stream mining (UDM) in mobile and distributed environments. Accessing and analyzing time critical data streams from a ubiquitous computing device offer many challenges. It requires a new breed of data mining algorithms that can handle continuous stream of data. In addition, UDM techniques should pay attention to the cost due to communication, computation, security, power consumption, and other factors. The tutorial will cover the following material: 1) Ubiquitous data mining: Introduction and motivation, 2) Accessing data streams in ubiquitous environments, 3) Data mining in a ubiquitous environment: An overview, 4) Cost of UDM: Systems, communication, power, security issues, 5) Data stream mining algorithms from single and multiple sources, 6) Communication languages for UDM applications, 7) Human-computer interaction issues, 8) Applications: Case studies, and 9) Future possibilities.

Lecturer: Dr. Kargupta is an Assistant Professor in the Department of Computer Science and Electrical Engineering, University of Maryland Baltimore County. He is also a cofounder of Agnik (http://www.agnik.com), a company specializing on ubiquitous data intelligence. He received his Ph.D. in Computer Science from University of Illinois at Urbana-Champaign in 1996. His research interests include mobile and distributed data mining and computation in gene expression.

Dr. Kargupta won the National Science Foundation (NSF) CAREER award in 2001 for his research on ubiquitous and distributed data mining. His research is also funded by several other grants from NSF, NASA, TRW Research Foundation, and Others. He won the 1997 Los Alamos Award for Outstanding Technical Achievement. His dissertation earned him the 1996 SIAM (Society for Industrial and Applied Mathematics) annual best student paper prize. He has published more than sixty peer-reviewed articles in journals, conferences, and books. He is the primary editor of a book entitled "Advances in Distributed and Parallel Knowledge Discovery", AAAI/MIT Press. He is an Associate Editor of the IEEE Transactions on System, Man, and Cybernetics, Part B. He has been in the Organizing Committee of the 2001, 2002, and 2003 SIAM International Data Mining Conference. He is a member of the program committee for the 2001 ACM SIGKDD conference and the 2002 IEEE International Conference on Data Mining, 2002 HiPC Conference, and 2002 CIKM among others. He organized numerous workshops, offered several tutorials, and edited journal special issues. More information about him can be found at http://www.cs.umbc.edu/~hillol.

9:00 am - 1:00 pm

TUTORIAL IV

The Early 21st-Century Processor Architecture Landscape

Sriram Vajapeyam
Independent Consultant

Audience: Any one interested in a quick but comprehensive overview of the current processor landscape and having (a) basic background in computer architecture and organization, and (b) some exposure to advanced processor architecture. The tutorial should be useful to a variety of people in the field, including decision makers, technical managers, practicing engineers, research students and faculty members.

Course Description: Processors today populate a variety of markets and application domains: the traditional high-end servers, desktop and mobile computers; embedded computers, especially DSPs, network processors, etc. Traditionally, the advanced micro-architectural features used in processors, within the von Neumann model framework, have trickled down from supercomputers to workstations to PCs. While this trend continues today with embedded processors, DSPs, etc., these newer domains also incorporate processor features and technologies specially suited for just their applications.

In this tutorial, we will provide a quick overview of this increasingly complex processor architecture landscape. We first identify and classify several basic processor micro-architectural techniques in the contexts of a typical general-purpose super-scalar processor model

and a vector processor model. Extensive speculative processing, multi-threading, modular and hierarchically decoupled instruction issue, and dynamic code optimization are some of the more important trends in traditional high-performance CPUs. Next, we will contrast the general-purpose workload's characteristics with those of the DSP and network processing domains. This will serve as a springboard for looking at the processors (micro-architectures) of those domains. For example, vector-style processing is an important feature in DSP processors. Throughout, we will highlight example features from commercial processors of the respective domains.

Finally, we will touch upon the exciting less-traditional aspects of the current processor landscape. Dynamic cross-platform binary translation (and code optimization) is breaking the traditional binary compatibility lock in general-purpose and high-end computing. The newer computing domains employ important technologies such as configurable/reusable IP cores, reconfigurable fabrics, system-on-chip, special-purpose co-processors, (automated) processor customization and specialization, etc. We will provide a quick glimpse of several of these technologies.

Overall, the tutorial attendee will get a bird's eye view of significant architectural and technological trends in processors for the different computing domains.

Lecturer: Sriram Vajapeyam is currently an independent consultant in computer architecture and systems. He holds a Ph.D. (1991) and an M.S. in Computer Science from the University of Wisconsin-Madison, and a B.Tech. in Electrical Engineering from IIT-Madras. Vajapeyam worked for a year at Cray Research ('91-'92) after his Ph.D., and has done a 6-month sabbatical at Analog Devices India, a 3-month Visiting Professorship at Intel Microprocessor Research Labs, and 8+ years in a faculty position in India. He has held several short-term visiting positions including at MIT, Univ. of Wisconsin, Cray Research, Univ. of Southern California (LA), and ACRI France. He has taught half a dozen tutorials at the top international computer architecture conferences (ISCA and ASPLOS) and written a guest-editorial on processors for IEEE Computer. Vajapeyam's research and professional interests are in computer architecture and systems.

9:00 am - 1:00 pm

TUTORIAL V

Wireless Sensor Network Protocols

Krishna M. Sivalingam
Washington State University

Audience: The tutorial is intended for practicing engineers in the networking and communications area. It is also very suitable for beginning graduate students with interests in wireless communication, networking, and mobile computing. Prior exposure to fundamentals of networking and wireless communication is a plus though not essential.

Course Description: Tremendous technological advances have been made in the development of low-cost sensor devices equipped with wireless network interfaces. The sensors monitor various types of information such as temperature, pressure, chemicals, etc. and/or transmit voice and video data. The design of large-scale sensor networks interconnecting several hundred to a few thousand sensor nodes has attracted recent research attention. Such sensor networks may be used for applications spanning several domains including military, medical, industrial, and home networks. The purpose of the tutorial is to present a comprehensive introduction to wireless sensor networks - basic concepts, challenges, recent research, and further possibilities. The topics covered will be based on fundamental concepts and up-to-date material in the literature, as listed below: 1) Introduction to wireless sensor networks and evolution of protocols for sensor networks, 2) Multiple Access Protocols, 3) Routing Protocols, 4) Energy-efficient protocol design, 5) Data querying, dissemination and fusion, 6) Security, 7) Testbeds and application scenarios, and 8) Summary: Future directions and unsolved problems in this research area.

Lecturer: Dr. Krishna Sivalingam received his Ph.D. and M.S. degrees in Computer Science from State University of New York at Buffalo in 1994 and 1990 respectively; and the B.E. degree in Computer Science and Engineering in 1988 from Anna University, Madras, India. He is currently an Associate Professor in the School of Electrical Engineering and Computer Science, at Washington State University, Pullman, where he was an Assistant Professor from 1997 to 2000. Earlier, he was an Assistant Professor at University of North Carolina Greensboro from 1994 until 1997. His research interests include wireless networks, optical wavelength division multiplexed networks, and performance evaluation. He has served as a Guest Co-Editor for a special issue of the IEEE Journal on Selected Areas in Communications on optical WDM networks. He is co-recipient of the Best Paper Award at the IEEE International Conference on Networks 2000 held in Singapore. He has published an edited book on optical WDM networks in 2000. He holds three patents in wireless networks and has published several research articles including more than twenty journal publications. He will be serving as General Co-Chair for SPIE Opticomm 2003 conference; and has served as Technical Program Co-Chair of SPIE/IEEE/ACM OptiComm conference at Boston, MA in July 2002, and as Workshop Co-Chair for Workshop on Wireless Sensor Networks and Applications (WSNA) to be held in conjunction with ACM MobiCom 2002 at Atlanta, GA in September 2002.

2:00 pm - 6:00 pm

TUTORIAL VI

Wireless Networking using IEEE 802.11 and Bluetooth: Technology and Research Challenges

Pravin Bhagwat
Indian Institute of Technology,
Kanpur and Winlab, Rutgers University
Rajeev Shorey
IBM India Research Lab. and
Indian Institute of Technology, New Delhi

Audience: This tutorial is intended for researchers and practitioners who want to track new developments in short range wireless communication, but who don't have time or patience to read all specifications. Computer professionals who want to develop better understanding of technology trends and identify new market opportunities in the area of wireless networking will also benefit from this tutorial. Basic understanding of layered network architecture is expected. No background in analog radio, signal processing, or wireless communication is required.

Course Description: The promise of untethered computing in the workplace is becoming a reality. IEEE 802.11b, the 11 Mbps wireless LAN standard, has finally arrived, and early market response has been positive. As the WLAN market takes off, Bluetooth, another emerging standard for short-range wireless networking, is also gathering force. Several vendors have demonstrated Bluetooth products, including cordless headsets, PCMCIA cards, and LAN access points. Both standards are competing for the same airwaves, but are they also chasing the same market? Will Bluetooth and 802.11b complement each

other, or will one technology eventually displace the other?
This tutorial will explain the key design aspects of IEEE 802.11 and Bluetooth standards and illustrate how technology innovation and market forces are shaping their evolution. We will begin with some basic concepts (RF, signal processing) and technology trends (low cost, low power, small form factor). We will then give an overview of 802.11b and the Bluetooth 1.1 specifications. This will be followed by a brief discussion of Wireless PANs and the IEEE 802.15.1 standard. The final part will be devoted to future directions and open research issues in Wireless LANs and Wireless PANs.

Lecturers: Pravin Bhagwat is an entrepreneur and a well-known researcher in the area of wireless and mobile networking. Currently, he is directing a large-scale 802.11 deployment project in India and also working as a visiting professor in the computer science department, IIT Kanpur. He was the principal architect at ReefEdge, Inc., a wireless networking infrastructure and software company based in NJ. He played an active role in the standardization of Bluetooth PAN profile and also served as the chair of the Internet Engineering Task Force BOF on IP over Bluetooth. Prior to working for ReefEdge, he worked as technology consultant in the Networking Research group at AT&T Labs-Research, and as a member of research staff at IBM Thomas J. Watson Research Center. He is the chief architect of BlueSky, an indoor wireless networking system for palmtop computers, and the co-inventor of TCP splicing, a technique for building fast application layer proxies. He received his Ph.D. in computer science from the University of Maryland, College Park.

Rajeev Shorey received the Bachelor of Engineering (B.E) degree in Computer Science from the department of Computer Science and Automation, Indian Institute of Science, Bangalore, India in 1987. He received the M.S and Ph. D degrees in Electrical Communication Engineering from the Indian Institute of Science, Bangalore, India, in 1990 and 1995 respectively. From December 1995 to February 1998, he was with Silicon Automation Systems (now Sasken), Bangalore, India where he worked in the performance modeling and analysis of CDMA networks. Since March 1998, he is a Research Staff Member in the IBM India Research Laboratory, Indian Institute of Technology, New Delhi, India. His research interests include wireless networks, Internet protocols, performance modeling and analysis of wireline and wireless networks. Dr. Shorey is in the technical program committee of several international conferences in networking, namely, IEEE Infocom 2002, IEEE Infocom 2003, IEEE ICC 2003, and IEEE Globecom 2002. He is an adjunct faculty in the department of Computer Science and Engineering, Indian Institute of Technology, New Delhi and is a senior member of IEEE.

2:00 pm - 6:00 pm

TUTORIAL VII

Quantum Computing

Rajendra K. Bera
IBM Global Services India Pvt. Limited

Audience: This tutorial is intended for educators, graduate students and researchers interested in pursuing quantum computing.

Course Description: Quantum computing is one of the fascinating technologies in development today. Although the technology has a long way to go before it matures and can be used to build computers for regular use, there have been some spectacular successes in terms of research results, both in hardware and in algorithm development. This tutorial will describe some of the recent advances made in quantum computing to a nonspecialist audience. The tutorial will cover the basic concepts of quantum mechanics (state vector and superposition of states, entanglement, decoherence, measurement, etc.) as applicable to quantum computing, quantum computers and basic operations on such computers, and quantum algorithms (Shor's factorization algorithm, and Grover's list search algorithm). Prior knowledge of quantum mechanics is not necessary.

Lecturer: Rajendra K. Bera received his B. Tech., M. Tech., and Ph. D. degrees in aerospace engineering from the Indian Institute of Technology, Kanpur. He was a researcher for over 20 years at the National Aerospace Laboratory, Bangalore, India; a visiting assistant professor of aerospace, mechanical, and nuclear engineering at the University of Oklahoma, USA (1979-80); and a visiting faculty of aerospace engineering at the Indian Institute of Technology, Kanpur, India (1988). He is a Fellow of the Institution of Engineers (India) and a member of the New York Academy of Sciences. He has published more than 30 research papers in refereed journals and has more than a dozen IBM US patents that are pending. Currently, he heads the R&D Group (Exports) of IBM Global Services India.

2:00 pm - 6:00 pm

TUTORIAL VIII

Design for High Reliability, Availability and Serviceability

Dhiraj K. Pradhan
University of Bristol

Audience: Engineers and Researchers

Course Description: This tutorial discusses the factors that cause system failure (hardware fault, noise, software bugs, etc.) and then presents the wide range of techniques, both hardware and software, that have been developed to protect the system from these threats. Also discussed are design techniques to enhance fault tolerance in multiprocessor distributed systems. This part concludes with a discussion of models for evaluating the effectiveness of these techniques in terms of reliability and availability improvements versus the hardware, software, and/or performance overhead.

Lecturer: Dhiraj K. Pradhan is currently a Chair Professor in the Department of Computer Science at the University Bristol (U.K.). Recently, he was a Professor in the Electrical & Computer Engineering Department of Oregon State University, in Corvallis. Previously, Dr. Pradhan held the COE Endowed Chair Professorship in Computer Science at Texas A&M University, in College Station, as well as serving as Visiting Professor at Stanford University, in California. Before that, Professor Pradhan was Professor/Coordinator of Computer Engineering at the University of Massachusetts, in Amherst, along with other positions.

Dr. Pradhan's contributions include two patents, serving as co-author/editor of several books, including Fault-Tolerance Computing: Theory & Techniques, Vol. I & II (Prentice-Hall, '86), Fault-Tolerant Computer Systems Design (Prentice-Hall, '98), IC Manufacturability: The Art of Process and Design Integration (IEEE Press, '99). Prof. Pradhan's honors include the '96 IEEE Transactions on Computer-Aided Design Best Paper Award; Fellow, ACM; Humboldt Distinguished Senior Scientist Award/ Germany; '97-'98 Fulbright-Flad Chair in Computer Science.

WEDNESDAY, DEC. 18

2:00 pm - 6:00 pm

TUTORIAL IX

Data Grid Management Systems: Towards Knowledge Grid Networks

Arcot Rajasekar and Arun Jagatheesan
San Diego Supercomputer Center
University of California, San Diego

Audience: Since the tutorial covers basics, open research issues and demonstration sessions, a wide variety of people fall into the category of "intended audience". Based on similar experiences before at NPACI (National Partnership for Advanced Computing Infrastructure), the following people would be benefited: Beginners, Students: The introductory sections will provide valuable information on Data Grids, Computational Grids and projects using these technologies. Researchers: Investigators who already are in HPC will be updated on new challenges and methodology in data management. System Developers: Information about data grid requirements and components will showcase future development challenges. Commercial Companies: The case studies would provide solutions to similar problems in the commercial world.

Course Description: Data grids handle large-scale, distributed, heterogeneous collections of data shared among virtual organizations. This tutorial provides insight into opportunities, components and case studies of data grids and explores their usage in high performance and large scale computing environments. Starting with challenges in data handling, the tutorial will also provide an overview of the data grid technology, design philosophy, best practices and services for the next generation commercial and scientific applications. It will introduce the burgeoning field of data grid management systems (DGMS), and illustrate real-life grids (GriPhyN, NVO, BIRN, etc.) and grid components (Storage Resource Broker, Grid Portal, etc.). If possible, a hands-on session to use and "feel" a working data grid system will be provided. The course outline is as follows: 1) Introduction to Data Grids (What?), 2) Requirement for Data Grids (Why?), 3) Data Grid Components (How?), 4) Case Studies (Where?), 5) SRB Demo/Hands On (Can I?), 6) Other Technologies (What else?), 7) Data Grid Management Systems, 8) Knowledge Grid Network (What next?), and 9) Uncharted Waters (New challenges?).

Lecturers: Dr. Arcot Rajasekar is the Director of the Data Grid Technologies Group at the San Diego Supercomputer Center at UCSD. His research interests include data grids, digital library systems, persistent archives and distributed data collection & metadata management. He is a key architect of the SDSC Storage Resource Broker, an intelligent data grid integrating distributed data archives, file repositories and digital collections. Dr. Rajasekar received his PhD from the University of Maryland and has more than 50 publications in artificial intelligence, databases and data grid systems. His email address is sekar@sdsc.edu.

Arun Jagatheesan is a Visiting Scholar at the San Diego Supercomputer Center and a member of the High Energy Physics Group at the University of Florida. His current research interests include Internet Computing, Data Grid Management, Semantic Web and Workflow Systems. He is involved in research and development of GriPhyN (Grid Physics Network), SRB Web Services and Data Grid Management Systems at SDSC. Jagatheesan received his M.S in Computer Science from the University of Florida. His email address is arun@sdsc.edu.

2:00 pm - 6:00 pm

TUTORIAL X

Opportunities and Challenges in Pervasive Computing

Raju Pandey
University of California, Davis

Audience: This tutorial is meant for core Computer Science researchers, educators and students, and applied computational sciences researchers (including engineers, environmental scientists, agriculture experts, and other application developers) who are interested in understanding the opportunities and challenges that pervasive computing environments offer.

Course Description: There is increasing interest in the next generation of distributed systems that include a large number of embedded sensors, actuators and MEMS devices. Such systems, called variously as pervasive, ubiquitous, or networks of embedded systems in literature, include heterogeneous collections of devices that are embedded in their physical environment and that interact with the environment, gather information, perform local computations, and communicate with other devices and hosts. Pervasive systems allows tight integration of the physical world with a computing system infrastructure, thereby permitting better information sensing, access, and control. The primary goal of this tutorial is to provide a comprehensive overview of the pervasive computing area to both Computer Science researchers and application developer community. For Computer Science researchers, this tutorial will address how characteristics of pervasive environments (such as resource constraints, connectivity and configuration, scalability, fault tolerance and security concerns) require novel solutions for many traditional distributed systems problems. For application developers, this tutorial will illustrate how this exciting technology can be used to build novel applications in agriculture, environmental sciences, engineering, medicine, disaster recovery and response, and smart computing environments. The tutorial is divided into four segments. First, it will discuss the computational, communication and sensor characteristics of the various devices currently available. Second, it will describe the networking techniques for constructing a communication infrastructure among ubiquitous devices. The tutorial will discuss several classes of sensor network routing algorithms, and their applicability within different application domains. Third, the tutorial will highlight the operating system, middleware, and programming language support needed for integrating a large number of devices into a secure, fault tolerant and adaptive distributed computing environment. Finally, the tutorial will discuss the issues in building and deploying new classes of applications within a pervasive computing environment.

Lecturer: Raju Pandey is an Associate Professor in the Department of Computer Sciences at University of California, Davis. He received his B. Tech degree in Computer Science and Engineering from the Indian Institute of Technology, Kharagpur in 1984, an M.S. in Computer Science from University of Massachusetts, Amherst, and a Ph. D. in Computer Science from the University of Texas at Austin in 1995. His research interests are primarily in distributed systems, operating systems, networking, and pervasive computing. Dr. Pandey is a member of ACM and a member of IEEE-CS.

LOCAL INFORMATION

Conference Site
December 18, 19, 20, and 21

Taj Residency
41/3, Mahatma Gandhi Road
Bangalore - 560 001
Karnataka, India
E-mail : residency.bangalore@tajhotels.com

Tel: +91-80-558-4444
Fax: +91-80-558-4748

Due to large number of activities on December 18, some tutorials will be held at an alternate location. Check the HiPC website for location information.

About Bangalore
Bangalore, a bustling metropolis, is the fifth largest city in India and the capital of the state of Karnataka. It is the main center of the Information Technology industry in India; almost every Indian and multi- national IT company has a presence here. Bangalore is home to the Indian Institute of Science (IISc), a premier research institute, and many other aerospace and high technology industries including the Centre for Development of Advanced Computing. Karnataka is home of many ancient Indian architectural marvels, wildlife sanctuaries, rain forests (the Western Ghats), pristine beaches, and rich and hoary cultural traditions.

Sightseeing Tour
There will be a local sightseeing tour following the conference. Tentative schedule: December 22, 7:00 am - 6:00 pm.

Please check the HiPC website for details.

Travel Checklist

Visa:
All non-Indian-citizens are required to have an Indian visa to enter the country. Please allow yourself sufficient time (say 2-3 weeks) to procure an appropriate visa from your nearest Indian consulate. Please check the conference website for information about Indian consulates.

Flight Reservations:
Flights to India tend to fill up well ahead of the December holiday season. We recommend that you make your flight reservations about 3-4 months in advance.

Vaccinations (shots):
Many first-time travelers to India prefer to get preventive vaccinations.

Foreign Exchange:
While international credit cards are widely accepted in commercial establishments in India, several places rely on cash transactions in the local currency (Indian Rupee). We suggest that you carry some Indian currency when entering India or buy Indian currency at the airport when you arrive. The current exchange rate is about Rs. 48/- per US dollar. Once in India, you can buy additional Indian currency from local branches of Citibank, Thomas Cook, etc. However, it is typically difficult to convert Indian currency back into foreign currency because of exchange regulations.

Hotel Reservations:
Please make your hotel reservations ahead of time so that you get your choice of accommodation. Check the conference website for information about accommodations. You may also find attractive rates on the web.

Time and Weather
The Indian Standard Time (IST) is 5 1/2 hours ahead of the Greenwich Mean Time(GMT) and is 13 1/2 hours ahead of the U. S. Pacific Standard Time(PST). In December/January the weather is mildly tropical with temperatures averaging about 21° Celsius (approx. 70° Fahrenheit) during the day and about 16° Celsius (approx. 60° Fahrenheit) during the night.

Sunrise – 6:06 am (approx.)
Sunset – 5:28 pm (approx.)

For detailed local information, visit the HiPC website at http://www.hipc.org/hipc2002. Check out the local info and accommodation sections.

Airport to Hotel Transportation
The airport is 6 kms (approx 3.5 miles) from Taj Residency. The taxi fare can vary. One way prepaid taxi fare is approximately Rs. 250 plus tip. You can book a taxi at the prepaid taxi counter of KSTDC which operates round the clock for passengers arriving by domestic and international flights. The counter is situated in Terminal II immediately after the baggage claim area.

High Performance Computing 2002
University of Southern California, EEB 200C
Los Angeles, CA 90089-2562, USA

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