HiPC 2015 Industry Birds-of-a-Feather Sessions

Speakers' Bios: Intel, AMD and SanDisk

Intel BoF Session Leaders' Bios:

James Reinders

Chief Evangelist and Author, Intel Software

James Reinders works to increase the use of parallel programming throughout the industry and has contributed to numerous projects including the world's first TeraFLOP/s supercomputer (ASCI Red) and the world's first TeraFLOP/s microprocessor (Intel® Xeon Phi™ coprocessor). James has authored and edited numerous technical books, including: Intel Threading Building Blocks (O'Reilly, 2007), Structured Parallel Programming (Morgan Kaufmann, 2012), Intel® Xeon Phi™ Coprocessor High Performance Programming (Morgan Kaufmann, 2013), Multithreading for Visual Effects (2014), High Performance Parallelism Pearls Volume One (Morgan Kaufmann, 2014) and the just released High Performance Parallelism Pearls Volume Two (Morgan Kaufmann, 2015).

Avinash Sodani

Chief Architect, "Knights Landing" Xeon-Phi processor at Intel Corporation

Avinash Sodani holds a PhD in Computer Architecture and an MS in Computer Science, both from University of Wisconsin-Madison and earned a B. Tech in Computer Science and Engineering from IIT Kharagpur in India. He is a Senior Principal Engineer at Intel Corporation. His work focuses on high performance computing and he leads the architecture for Xeon-Phi processors. He is the chief architect of the future Xeon-Phi processor, Knights Landing, with responsibility for the processor's overall architecture and definition. Previously, he was one of the primary architects of the 1st generation Core i7/i5/i3 processor, called Nehalem, where he was responsible for the architecture of the "Out-of-order schedule" cluster of the Core. Avinash has worked as a server architect for the Xeon line of products, covering Westmere servers and early work on Haswell servers. He has also worked briefly as a system architect for a processor targeting game consoles.

Dr. Avinash Palaniswamy -Nash

Senior Manager Throughput Computing, Intel, USA

Dr. Nash has been at Intel since October 2005, and his focus is in the areas of High-End HPC and Throughput Computing in the Datacenter group. His responsibilities include the strategy and marketing efforts around High-End HPC hardware and software solutions, Intel® QuickAssist Technology enabled Accelerators, and other technologies related to throughput computing. His prior responsibilities at Intel included being the World Wide Web Consortium Advisory Committee representative from Intel. Prior to joining Intel as part of the acquisition of Conformative Systems, an XML Accelerator Company, he has served in several senior executive positions in the industry including being the Director of System Architecture at Conformative Systems, CTO/VP of Engineering at MSU Devices, and Director of Java Program Office and Wireless Software Strategy in the Digital Experience Group of Motorola, Inc. Dr. Palaniswamy holds a B.S. in Electronics and Communications Engineering from Anna University (Chennai, India) and an M.S. and Ph.D. from the University of Cincinnati in Electrical and Computer Engineering.

AMD BoF Speaker Bio:

Gandham Phanikumar

Indian Institute of Technology Madras

Currently a Professor in the Department of Metallurgical Materials Engineering at Indian Institute of Technology Madras, Gandham Phanikumar has been a faculty member since 2005. He teaches courses on Transport Phenomena, Solidification, Thermodynamics, Material Characterization and Welding and specialises in the areas of Solidification and Welding with an emphasis on the high performance aspects of micro structure simulation techniques. Gandham holds a Ph.D. from Faculty of Engineering, Indian Institute of Science, Bangalore, and was a post-doctoral fellow with a scholarship from Alexander von Humboldt Foundation at the German Aerospace Center, Cologne.

SanDisk BoF Speaker Bio:

Dr. Pankaj Mehra

VP and Senior Fellow at SanDisk

Pankaj Mehra is VP and Senior Fellow at SanDisk, through the acquisition of Fusion-io where he was SVP & CTO. A graduate of the first CSE batch from IITD, Pankaj obtained Ph.D. (CS) from The University of Illinois at Urbana-Champaign. He has served on the faculty of IIT Delhi and UC Santa Cruz, and been a faculty visitor to IBM. With three books and more than 50 published papers and patents in topics ranging from high performance computing to artificial intelligence, Pankaj's experience spans multiple areas of computer science and spans experience in academia, government, and industry. He has founded two companies and is one of the authors of InfiniBand 1.0 specification, where he chaired the Management Working Group. His work has been recognized with awards from NASA and Sandia National Labs, and his system designs in the 90s held TPC-C and TeraByte Sorting performance records. Pankaj's inventions include persistent memory, virtual switch, and compression-enhancing routing algorithms.