22nd IEEE International Conference on High Performance Computing

Bengaluru (Bangalore), India • December 16-19, 2015

PROGRAM OVERVIEW

Starting on Wednesday, December 16th, the first day of HiPC 2015 will feature a Student Research Symposium (SRS) and four Workshops. The day will conclude with an Industry Gala. The main technical program, held on Days 2, 3 and 4, will feature three invited keynote speakers and eight single track sessions of peer reviewed papers. An Academic BoF will be held on Day 2 and another on Day 4. On Days 2 and 3, there will be a full program of the Industry Exhibition and related industry events including two Industry, Research and Users Symposium (IRUS) sessions and five Industry BoFs.

KEYNOTE SPEAKERS

Thursday, December 17th – Day 2 Keynote

Scale-Out Beyond Map-Reduce

Raghu Ramakrishnan
Head, Big Data Engineering &
Head, Cloud Information Services Lab
Microsoft

Friday, December 18th – Day 3 Keynote

Compilers and the future of high performance computing

David Padua
Donald Biggar Willet Professor of Computer Science
University of Illinois at Urbana-Champaign

Saturday, December 19th – Day 4 Keynote

The Architecture of Smart Phones

Trevor Mudge
Bredt Family Professor of Engineering
University of Michigan

TECHNICAL PROGRAM

The HiPC 2015 technical program on Days 2, 3 and 4 will consist of 48 peer reviewed papers chosen from over 200 submissions from all over the world. The papers will be presented in eight single-track sessions and will cover important and timely topics in all areas of high performance computing. The three keynote speakers will open the morning plenary sessions.

WORKSHOPS

Four workshops covering diverse topics complementary to the conference technical program will be held on Day 1 of the conference in parallel to the Student Research Symposium. They have been shaped as half-day event and will focus on:

1. *Computational Fluid Dynamics (CFD);*
2. *Foundations of Big Data Computing;*
3. *InfoSymbiotics/ Dynamic Data Driven Applications Systems (DDDAS) for Smarter Systems;*
4. *Architectural Support and Middleware for InfoSymbiotics/DDDAS.*

Papers from Workshops 1 and 2 are included in the proceedings, and the abstracts from Workshops 3 and 4 are also part of the proceedings to be distributed at the conference.

STUDENT RESEARCH SYMPOSIUM

Held on Day 1 of the conference, the 8th Student Research Symposium (SRS) will feature brief presentations by student authors on their research, followed by a poster exhibit. The SRS program will also include short talks by leading HPC experts: Raghu Ramakrishnan from Microsoft whose talk is titled *Big Data@Microsoft* and Vianney Koelman from Shell whose talk is titled *Bits, Bytes, Barrels: HPC in the Energy Industry.* Following lunch, there will be an author workshop for students. At the end of the day, the conference reception will provide an opportunity for students to interact with HPC researchers and practitioners from academia and industry.

ACADEMIC BoF SESSIONS

Two Academic Birds-of-a-Feather (BoF) sessions will be held on Day 2 and Day 4 of the conference. The scheduled topics are:

1. *Compilation Research using LLVM*
2. *Advanced Numerical Schemes for Massively Parallel Computing: Challenges and Opportunities*

Organized by academic and non-commercial research groups, these two-hour sessions will focus on emerging areas of interest and will provide a forum for discussion to help stimulate new research ideas, address specific problems, and build a research community in the topic area. They can also serve as the point of origin for future conference workshops.

INDUSTRY EVENTS

The conference welcomes (and strongly encourages) industry participation on all days at all levels including in the technical program and student symposium. The industry/research exhibition, to be held on December 17th and 18th, will include booths and demonstrations and will showcase products, services and current work from vendor companies and R&D laboratories. **Two Industry, Research and Users Symposium (IRUS) sessions** on the topics related to Computational Science & HPC will be held on Day 2 and will bring together solution providers and users of HPC in a forum to discuss platforms and technologies and best practices. **Industry supporting sponsors will host five BoF's** on Days 2 and 3 of the conference.

WELCOME TO HiPC 2015

All HiPC sponsored events during the four days of HiPC are open to all registrants. This year the proceedings of the conference will include the four workshops to be held on Day 1. Produced by the Conference Publishing Services (CPS) of the IEEE Computer Society, the proceedings will be distributed online in two volumes with separate ISBNs for the conference technical program (HiPC 2015) and for the workshops (HiPC W 2015). A thumb drive of the online proceedings will be available for purchase at registration.

If you have questions or need directions, please go to the "May I Help You" sign at Registration. You may be able to answer the question by checking the Website pages online or reviewing the following pages. Please note that the information that follows in this program was taken from several sources so apologies in advance to anyone who has not been correctly listed.

Conference attendees will also have access to a Mobile App, hosted by CPS. Details will be sent via email to all registrants, along with instructions for accessing the online proceedings. This participant handbook and the HiPC website should have all of the information needed to learn details of events and to navigate the schedule and location of events, and the HiPC Mobile App will give you instant access to the same information plus any updates on the conference.

- **To HiPC 2015 Supporting Industry and Organizations**
  The HiPC 2015 organizers wish to thank the 2015 companies for their generous support of the conference. This makes it possible to include in our proceedings the contributions of government and academic researchers and faculty and students from all over India.

- **To HiPC 2015 Attendees**
  We also appreciate the many top researchers in high performance computing from all over the world who attend and participate in this forum along with colleagues from leading Indian research labs and Indian academic institutions. We hope that everyone attending this year can plan to join us in 2016 when HiPC will be held in Hyderabad on December 19-22. Watch the Website and your inbox for information on plans for next year.

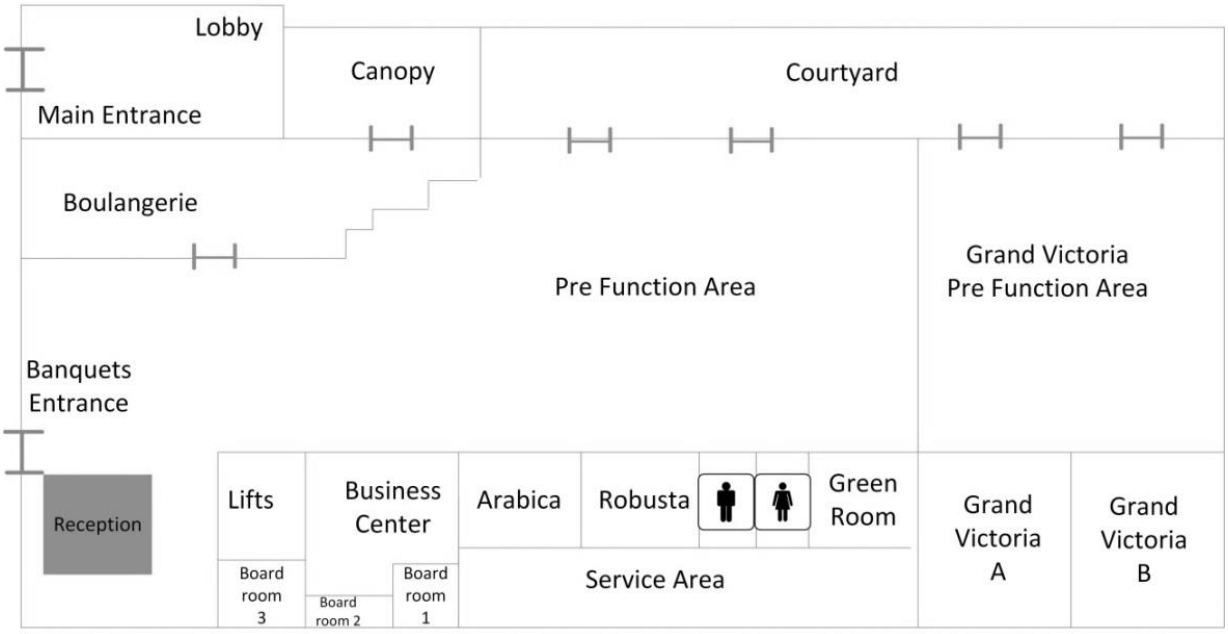
- **At the conclusion of the conference**
  Before you depart the conference or after, please take a few minutes to provide online feedback to HiPC organizers so that we know what kind of improvements we can make for next year. The HiPC 2015 Volunteers who have organized this year's event are listed at the end of this book, and they will appreciate any constructive comments you have about your experience this year.

LOCATION & SCHEDULE OF EVENTS

The next two pages have full information on the meeting space and where events will be held – where, what and when! The pages that follow give details on all events including speakers and their topics and the titles and authors of papers to be presented. All information is organized by day of the conference: Day 1 through Day 4. Any changes will be posted at the registration desk.

CONFERENCE VENUE & LOCATION OF EVENTS

Park Plaza Bengaluru Hotel
Meeting Rooms & Foyer Areas



There are four main meeting rooms in the conference venue. They are **Arabica** and **Robusta**, next to each other; and the **Grand Victoria A & B** halls, which combined are where the keynotes and the Friday evening banquet will be held. The Industrial Exhibits will be located in the **pre-function areas outside the meeting rooms**, and the registration area is near the Reception area. On Day 3, **Sponsor Feedback meetings** will be held in Arabica. Any **changes in the location of events will be posted** near the registration area. The following is the scheduled location of events:

	Arabica	Grand Victoria A	Grand Victoria B	GV A+B
Day 1	Workshops 3 & 4	SRS Sessions & Posters	Workshops 1 & 2	
Day 2		Technical Sessions 1-2-3 + Fujitsu I-BoF	IRUS 1 & 2 + AcBoF-1	Keynote
Day 3	Shell I-BoF	Technical Sessions 4-5-6	Intel, AMD, SanDisk BoFs	Keynote + Banquet
Day 4		Technical Sessions 7-8	AcBof-2	Keynote

Registration opens at 7:00 AM on all four days of the conference, with breakfast available in the Foyer the hour before events start. There will be mid-morning and mid-afternoon coffee/tea/snacks **breaks and lunch on all four days**. Break and lunch times vary by day. See the full schedule that follows for times.

HiPC 2015 PROGRAM DAILY SCHEDULE

Please check the Website and postings at the venue for up-to-date information on locations and schedules for each event. The following shows start times.

Start Time	DAY 1	DAY 2	DAY 3	DAY 4
	Wednesday, 16 Dec	Thursday, 17 Dec	Friday, 18 Dec	Saturday, 19 Dec
All Day		•Industrial Exhibits	•Industrial Exhibits	
7:00 AM	Registration_____	•Registration_____	Registration_____	Registration_____
7:30	BREAKFAST	•BREAKFAST	BREAKFAST	BREAKFAST
8:00		HiPC 2015 Opening		
8:30	•SRS	Keynote	Keynote	Keynote
9:00	•WORKSHOP 1 •WORKSHOP 3	RAGHU RAMAKRISHNAN	DAVID PADUA	TREVOR MUDGE
9:30		BREAK	BREAK	BREAK
10:00		•Technical Session 1 •IRUS 1	•Technical Session 4 •Industry BoF-INTEL •Industry BoF-SHELL	•Technical Session 7 •Academic BOF-2
10:30	BREAK			
11:00	•SRS			
11:30	•WORKSHOP 1 •WORKSHOP 3			
12:00 PM		LUNCH	LUNCH	LUNCH
12:30				
1:00	LUNCH		•Technical Session 5 •Industry BoF-AMD	
1:30		•Technical Session 2 •IRUS 2		•Technical Session 8
2:00	•SRS Author Workshop			
2:30	•WORKSHOP 2 •WORKSHOP 4			
3:00			BREAK	
3:30		BREAK	•Technical Session 6 •IndustryBOF-SanDisk	Conference Closes
4:00	BREAK •SRS Posters (set up)	•Technical Session 3 •Academic BOF-1		
4:30	•WORKSHOP 2			
5:00	•WORKSHOP 4			
5::30	•SRS Posters (on display)		BREAK	
6:00		Awards		
6:30	•SRS Posters & Hi Tea	BREAK		
7:00	•Industry Gala	•Industry BoF-Fujitsu	• Cultural Program	
7:30				
8:00			•Banquet	
8:30				
9:00				
9:30 PM				

2016

December 19-22, 2016

Hyderabad, India

Day 1 - Wednesday, December 16

Breakfast @ 7:00, Breaks @ 10:30 and 4:00, Lunch @ 1:00

Student Research Symposium (SRS)

Starts at 8:30 AM – Wednesday, December 16th

The 8th **student research symposium** on High Performance Computing (HPC) is aimed at stimulating and fostering student research, and providing an international forum to highlight student research accomplishments. It features brief presentations by student authors on their research, followed by a **poster exhibit in the evening**, which will include the papers presented in the morning symposium. Those papers and posters are listed below and will be on display as part of the poster session during the HiPC Reception and **Industry/Faculty/Students Mixer**. Leading HPC researchers/practitioners will be present to offer comments and interact with the student presenters.

8:40 AM: Keynote Talk 1

Big Data@Microsoft

Raghu Ramakrishnan (Microsoft)

9:40 AM SRS Papers: Session 1

D-face: Parallel implementation of CNN based Face Classifier using Drone Data on K40 & Jetson TK1
Kaliuday Balleda (MulticoreWare, Inc, India); Pallav Kumar Baruah (Sri Sathya Sai Institute of Higher Learning, India); Sairam Menon (MulticoreWare, Inc, India); Harish Kumar, Ayyappa Theegala and Santosh Chaitanya (Sri Sathya Sai Institute of Higher Learning, India)

Dynamic Shortest Paths using JavaScript on GPUs
Anurag Ingole and Rupesh Nasre. (IIT Madras, India)

Multiscale multiphysics process on a HPC infrastructure: Application to coral growth process
Karthik Senthil (National Institute of Technology Karnataka, India); Paul Albuquerque (University of Applied Sciences of Western Switzerland, Switzerland); Jonas Latt (University of Geneva, Switzerland)

11:00 AM SRS Papers: Session 2

Parallelization of Depth-First Traversal using Efficient Load Balancing
Vsn Rayasam (Indian Institute of Technology Madras, India); Rupesh Nasre (IIT Madras, India)

Performance Improvement for Multi-Key Quick Sort using Kepler GPUs
Bharath Shamasundar (NMAM Institute of Technology, India); Amoolya Shetty (Vishveshwaraiya Technology University & NMAM Institute of Technolgy, India); Ananya Rao (Vishveraiya Technological University, Belgaum & NMAM Institute Of Technology, Nitte, India); Supreetha Shetty and Neelima Bayyapu (NMAM Institute of Technology, India)

Simultaneous Solving of Linear Programming Problems in GPU
Amit Gurung, Binayak Das and Rajarshi Ray (National Institute of Technology Meghalaya, India)

Answering "If-What" Questions to Manage Batch Systems
Sainath Batthala (Indian Institute of Technology, Indore & Tata Research Development and Design Center, Pune, India); Neminath Hubballi (Indian Institute of Technology Indore, India); Maitreya Natu (Tata Research Development and Design Center, India); Vaishali P Sadaphal (Tata Research, India)

12:00 PM: Keynote Talk 2

Bits, Bytes, Barrels: HPC in the Energy Industry

Vianney Koelman (Shell)

HiPC 2015 WORKSHOP 1:
Computational Fluid Dynamics (CFD)

8:30 AM: Opening of CFD Workshop

8:45 AM: Keynote Talk
Sanjay Mittal (IIT Kanpur)

09:30 AM: Technical Paper Presentations

On the Navier-slip boundary condition for computation of impinging droplets
Jagannath Venkatesan and Sashikumaar Ganesan (Supercomputer Education and Research Centre, Indian Institute of Science, Bangalore, India)

Development and Application of Interfacial Anti-Diffusion and Poor Mech Numerics treatments for Free Surface Flows
Vinay Kumar Gupta, Mohib Khan and Hemant Punekar (ANSYS Fluent India Pvt. Ltd., Pune, India)

11:00 AM: Technical Paper Presentation

Integrated Moisture Separator Design Using CFD
Girish Gowda and Balaji Kasturirangan (Research and Development, ELGI Equipments Ltd., Bangalore, India)

11:30 AM: Invited Talk
Anand Deshpande (Intel)

12:15 PM: Panel Discussion

12:45 PM: Closing Remarks

HiPC 2015 WORKSHOP 3:
InfoSymbiotics/Dynamic Data Driven Applications Systems (DDDAS) for Smarter Systems

9:00 AM: Welcome and Introductions

9:15 AM: Keynote Talk
Large-Scale Dynamic data and Large-Scale Big Computing for Smart Systems
Dr. Frederica Darema (Air Force Office of Scientific Research, USA)

10:45 AM: Technical Presentations (Abstracts)

An Efficient Parallel Implementation of the Ensemble Kalman Filter Based on Shrinkage Covariance Matrix Estimation
Elias D. Nino-Ruiz and Adrian Sandu (Virginia Tech, USA)

Stochastic Dynamics Modeling and Reduction for Predicting Phenomena Behavior in a Dynamic, Data-Driven Application System
Isaac J. Sledge and Kamran Mohseni (University of Florida)

A DDDAS CO Monitoring System: An Experimental Exploration
Matthew Silic and Kamran Mohseni (University of Florida, USA)

Distributed DDDAS through Receding Horizon Control
Vijay Gupta, Gregory Madey and Christian Poellabauer (University of Notre Dame, USA)

High Performance Processing of Streaming Data
Supun Kamburugamuve, Milinda Pathirage, Saliya Ekanayake and Geoffrey C. Fox (Indiana University, USA)

Design and Evolution of Cyber Physical Systems: A Dynamic Data Driven Application System
Sandeep Neema, Ted Bapty, and Jason Scott (Vanderbilt University, USA)

A dynamic data-driven approach to closed-loop neuroprosthetics based on multiscale biomimetic brain models
Salvador Dura-Bernal, Samuel A Neymotin, and William W Lytton (SUNY Downstate Medical Center, Brooklyn, USA); Amit Majumdar and Subhashini Sivagnanam (University of California San Diego, USA)

Starting at 2:00 PM –SRS Author Workshop

Starting at 4:00 PM –Posters on display in Multi-Function area

Starting at 6:30 PM – HiPC Reception and Mixer with Student Symposium Poster Exhibits

SRS Poster Session (includes papers presented above)

A Robust and Secure Cloud-Based RFID Authentication Protocol
Mrudula Sarvabhatla (NBKR IST, India); Chandra Sekhar Vorugunti (Dhirubhai Ambani Institute of Information and Communication Technology, India)

Balancing Energy with Routing Strategies using Secure Routing Protocol in Wireless Sensor Networks
Roopashree Patil and Basavaraj S Mathapati (Appa Institute of Engineering and Technology, India)

Scalability Analysis of Neural Networks and Extreme Learning Machines on Multi-Core Systems
Sanket Gupte and Dharm Jain (BITS Pilani, India)

Scaling up Training of Deep BLSTM Networks for Handwritten Text Recognition
Chebrolu VishnuVardhan (Sri Sathya Sai Institute Of Higher Learning, India); Vedavyasa Dhanireddy (Sri Sathya Institute of Higher Learning, India); Pallav Kumar Baruah (Sri Sathya Sai Institute of Higher Learning, India); Sai Rajeshwar Mudumba (Xerox Research Center, India)

SWIFT: A Fast Enhanced String Matching Algorithm for Heterogeneous Architectures
Sourabh S Shenoy (Vishveshwaraiya Technological University, India); Supriya Nayak, Udma (Visvesvaraya Technological University, India); Bayyapu Neelima (National Institute of Technology-karnataka Surathkal, India)

HiPC 2015 WORKSHOP 2:
Foundations of Big Data Computing

2:00 PM: Opening Remarks

2:10 PM: Keynote Talk
Big Data in Life Sciences and Public Health
Srinivas Aluru (Georgia Tech)

3:00 PM: Technical Paper Presentations

Performance Assurance Model for HiveQL on Large Data Volume
Amit Sangroya and Rekha Singhal

Scaling Computation on GPUs Using Powerlists
Anshu S Anand and Rudrapatna Shyamasundar

4:30 PM: Technical Paper Presentations

JL Lemma Based Dimensionality Reduction: On Using CDS Based Partial Fourier Matrices
Snigdha Tariyal, Narendra N and Girish Chandra

Sequential Multilinear Subspace based Event Detection in Large Video Data Sequences
Bharat Venkitesh, Pavan Kumar Reddy K and M Girish Chandra

5:10 PM: Panel Discussion

HiPC 2015 WORKSHOP 4:
Workshop on Architectural Support and Middleware for InfoSymbiotics/ DDDAS

2:00 PM: Technical Presentations (Abstracts)

Characterizing Distributed Stream Processing Systems for IoT Applications
Anshu Shukla, Tarun Sharma and Yogesh Simmhan (SERC, Indian Institute of Science, Bangalore, India)

Online Performance Model Learning to Minimize Performance Interference in Cloud Computing Infrastructure
Hamzah Abdel-Aziz, Faruk Caglar, Shashank Shekhar, Michael Walker, Xenofon Koutsoukos and Aniruddha Gokhale (Vanderbilt University, USA)

Scalability Aware Performance AutoTuning for OpenMP Applications
Shajulin Benedict, Rejitha R.S, and Suja A.Alex (HPCCLoud Research Laboratory, SXCCE, India)

Empowering the Next Generation City-Scale Smart Systems
Shashank Shekhar, Subhav Pradhan, Fangzhou Sun, Abhishek Dubey, Annirudha Gokhale (Vanderbilt University, USA)

DDDAS-based Resilient Cyber Battle Management Services (D-RCBMS)
Salim Hariri, Cihan Tunc, Pratik Satam and Firas Al-Moualem (University of Arizona, Tucson USA); Erik Blasch (Air Force Research Lab, Information Directorate, Rome, NY, USA)

Secure Privacy-Preserving DDDAS/Infosymbiotics Systems
Li Xiong and Vaidy Sunderam (Emory University, Atlanta, US

4:30 PM: Panel Discussion
Systems and Applications Synergies in InfoSymbiotics/DDDAS
Panelists: Frederica Darema, Aniruddha Gokhale, Adrian Sandu

5:30 PM: Closing Remarks

Day 2 - Thursday, December 17

Breakfast @ 7:00, Breaks @ 9:30 and 3:30, Lunch @ 12:00

8:00 AM – 8:30 AM Thursday, December 17

Plenary Session: Conference Inauguration and Opening Remarks

8:30 AM – 9:30 AM

HiPC 2015 Keynote Presentation 1:
Scale-Out Beyond Map-Reduce

Speaker: Raghu Ramakrishnan
(Head, Big Data Engineering & Head, Cloud Information Services Lab, Microsoft)

Abstract: Until recently, data was gathered for well-defined objectives such as auditing, forensics, reporting and line-of-business operations; now, exploratory and predictive analysis is becoming ubiquitous, and the default increasingly is to capture and store any and all data, in anticipation of potential future strategic value. These differences in data heterogeneity, scale and usage are leading to a new generation of data management and analytic systems, where the emphasis is on supporting a wide range of very large datasets that are stored uniformly and analyzed seamlessly using whatever techniques are most appropriate, including traditional tools like SQL and BI and newer tools, e.g., for machine learning and stream analytics. These new systems are necessarily based on scale-out architectures for both storage and computation. Hadoop has become a key building block in the new generation of scale-out systems. On the storage side, HDFS has provided a cost-effective and scalable substrate for storing large heterogeneous datasets. However, as key customer and systems touch points are instrumented to log data, and Internet of Things applications become common, data in the enterprise is growing at a staggering pace, and the need to leverage different storage tiers (ranging from tape to main memory) is posing new challenges, leading to caching technologies, such as Spark. On the analytics side, the emergence of resource managers such as YARN has opened the door for analytics tools to bypass the MapReduce layer and directly exploit shared system resources while computing close to data copies. This trend is especially significant for iterative computations such as graph analytics and machine learning, for which MapReduce is widely recognized to be a poor fit. I will examine these trends, and ground the talk by discussing the Microsoft Big Data stack.

10:00 AM – 6:00 PM Thursday, December 17 and Friday, December 18

Industry/Research Exhibition

Below are the companies who will be providing exhibits and demonstrations at HiPC 2015. Attendees are invited to visit booths and check posted schedules for demonstrations and talks and collect materials these exhibitors have prepared for the conference.

Allenia	Google	NetApp	RSC Group
Acer	G.T. Enterprise	Netweb	SanDisk
AMD	Intel	Nvidia	Shell
Fujitsu	Mellanox	Quantum	TATA

10:00 AM – 12:00 PM Thursday, December 17

Technical Session 1: Resilience and Customization

Which Verification for Soft Error Detection?
Leonardo Bautista-Gomez (Argonne National Laboratory, USA); Anne Benoit and Aurelien Cavelan (ENS Lyon, France); Saurabh Kumar Raina (Jaypee Institute of Information Technology, India); Yves Robert and Hongyang Sun (ENS Lyon, France)

Throughput Regulation in Shared Memory Multicore Processors
Xinwei Chen, He Xiao, Yorai Wardi, and Sudhakar Yalamanchili (Georgia Institute of Technology, USA)

Application Taxonomy via Algorithmic Commonality for Domain-specific Architecture Design
Yuanrong Wang and Qiangqiang Li (University of Chinese Academy of Sciences, P.R. China); Guangming Tan (Institute of Computing Technology, Chinese Academy of Sciences, P.R. China)

FlexCore: A Reconfigurable Processor Supporting Flexible, Dynamic Morphing
Furat Afram and Kanad Ghose (State University of New York at Binghamton, USA)

High Efficiency Generalized Parallel Counters for Xilinx FPGAs
Burhan Khurshid and Roohie Naaz (National Institute of Technology, Srinagar, India)

2QW-Clock: An efficient SSD buffer management algorithm
Dan He (Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology & Nanchang Hangkong University, P.R. China); Fang Wang, Dan Feng, Jing Ning Liu, and Yun Xiang Wu (Wuhan National Laboratory for Optoelectronics, Huazhong University of Science, P.R. China); Yang Hu (China Ship Development & Design Center, Wuhan, China); Ying He (Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology & Nanchang Hangkong University, P.R. China)

1:30 PM – 3:30 PM Thursday, December 17

Technical Session 2: Numerical and Combinatorial Algorithms

Task-based multifrontal QR solver for GPU-accelerated multicore architectures
Emmanuel Agullo (INRIA / LaBRI, France); Alfredo Buttari (CNRS - IRIT Toulouse, France); Abdou Guermouche (Université de Bordeaux, France); Florent Lopez (Université Paul Sabatier, France)

Structural Agnostic SpMV: Adapting CSR-Adaptive for Irregular Matrices
Mayank Daga and Joseph L. Greathouse (AMD Research, Advanced Micro Devices, Inc., USA)

On the resilience of parallel sparse hybrid solvers
Emmanuel Agullo, Luc Giraud and Mawussi Zounon (Inria, France)

New Tridiagonal Systems Solvers on GPU architectures
Adrián P. Diéguez, Margarita Amor and Ramón Doallo (University of A Coruña, Spain)

A Stable Parallel Algorithm for Diagonally Dominant Tridiagonal Linear Systems
S. Chandra Sekhara Rao and Rabia Kamra (Indian Institute of Technology Delhi, India)

Optimizing Approximate Weighted Matching on Nvidia Kepler K40
Md Naim and Fredrik Manne (University of Bergen, Norway); Mahantesh Halappanavar and Antonino Tumeo (Pacific Northwest National Laboratory, USA); Johannes Langguth (Simula Research Laboratory, Norway)

4:00 PM – 6:00 PM Thursday, December 17

Technical Session 3: High-end Software

Improving Communication Throughput by Multipath Load Balancing on Blue Gene/Q
Huy Bui (University of Illinois at Chicago, USA); Preeti Malakar, Venkatram Vishwanath, Todd Munson and Eun-Sung Jung (Argonne National Laboratory, USA); Andrew E Johnson (University of Illinois at Chicago, USA); Michael Papka (Argonne National Laboratory, USA); Jason Leigh (University of Hawaii at Manoa, USA)

Dynamic Adaptation for Elastic System Services using Virtual Servers
Abhishek Kulkarni (Indiana University, USA); Hugh Greenberg and Michael Lang (Los Alamos National Laboratory, USA); Andrew Lumsdaine (Indiana University, USA)

Understanding the Benefits of Asynchronous Data Transfers in Media Processors
Nagendra Gulur and Suriya Narayanan L (Texas Instruments, India)

Hardware-Transactional-Memory Based Speculative Parallel Discrete Event Simulation of Very Fine Grain Models
Emanuele Santini, Mauro Ianni, Alessandro Pellegrini, and Francesco Quaglia (DIAG–Sapienza Università di Roma, Italy)

Towards Practical Page Placement for a Green Memory Manager
Ashish Panwar and Kanchi Gopinath (Indian Institute of Science, India)

Efficient Barrier Implementation on the POWER8 Processor
C. D. Sudheer (IBM IRL, India); Ashok Srinivasan (Florida State University, USA)

10:00 AM – 12:00 PM Thursday, December 17

IRUS 1: Industry, Research, and User Symposium
Computational Science & HPC Track I

Academic and R&D Labs Speakers:

- Prof. S.M.Deshpande, Senior Research Associate, JNCASR, Bangalore
- Mr. Mandar Kulkarni, Tata Consultancy Services Limited
- Dr. Dipankar Das, Intel labs

Industry Track:
CRAY Inc.: To be announced

Q&A and Discussion

1:30 PM - 3:30 PM Thursday, December 17

IRUS 2: Industry, Research, and User Symposium
Computational Science & HPC Track II

Academic and R&D Labs Speakers:

- Prof. Sourendu Gupta, Theoretical Physicist, Tata Institute of Fundamental Research
- Dr. Atul Kumar Sahai, Scientist G, Indian Institute of Tropical Meteorology
- Prof. Sunil Sherlekar, CEO, Sankhya Sutra Labs, JNCASR

Industry Track:
NVIDIA : Marc Hamilton

Q&A and Discussion

4:00 PM – 6:00 PM Thursday, December 17

Academic Birds-of-a-Feather 1:
Compilation Research using LLVM

Abstract: This is an academic "birds of a feather" event on compilation research using the LLVM infrastructure. The Low Level Virtual Machine (LLVM) compiler is increasingly being used as the vehicle to develop compiler analysis and optimization infrastructure both in the industry and the academia. Several research groups in India academia have also started using LLVM, and some are actively contributing to it. The objective of this BoF is to disseminate information on existing efforts using LLVM in India, make the community aware of existing opportunities for research as well as software development, share experience and expertise in using LLVM for academic research, and instigate collaboration between groups. One of this BoF's goals is also to evolve into a full-fledged workshop in the next three years. For more details and program schedule, please visit the ABoF website.

Organizers and Program Chairs

- Uday Reddy B, Indian Institute of Science
- Dibyendu Das, AMD

Industry Birds-of-a-Feather (BoF) Sessions

Scheduled – Thursday, December 17

7:00-9:00 PM	**Fujitsu:** *Fujistu Forza, HPC Simplified (Ashok Chaudhry)*

Scheduled – Friday, December 18

10:00-12:00 PM	**INTEL:** *Need to Modernize Legacy Code? Panel of Intel Leaders in High End HPC hardware and software solutions ((James Reinders, Avinash Sodani, and Avinash Palaniswamy –Nash)*
10:00-12:00 PM	**SHELL:** *From Data to Knowledge: Converting Data to Actionable Insights*
1:00-3:00 PM	**AMD:** *Opportunities for GPU Computing in Integrated Computational Materials Engineering (Prof. Gandham Phanikumar, Department of Metallurgical and Materials Engineering, Indian Institute of Technology Madras)*
3:30-5:30 PM	**SanDisk:** *Contemplating a new memory hierarchy: a personal journey through persistent memory technologies (Dr. Pankaj Mehra, VP and Senior Fellow at SanDisk)*

Day 3 - Friday, December 18

Breakfast @ 7:00, Breaks @ 9:30 and 3:00, Lunch @ 12:00 (1 hour)

08:30 AM – 09:30 AM Friday, December 18

HiPC 2015 Keynote Presentation 2:
Compilers and the future of high performance computing

Speaker: David Padua
(Donald Biggar Willet Professor of Computer Science, University of Illinois at Urbana-Champaign)

Abstract: Compiler technology has enabled the software advances of the last sixty years. It has given us machine-independent programming and improved productivity by automatically handling a number of issues, such as instruction selection and register allocation. However, in the parallel world of high performance computing, the impact of compiler technology has been small. Part of the reason is that the ambitious research projects of the last few decades, such as automatic parallelization and automatic generation of distributed memory programs à la High Performance Fortran, are yet to produce useful results. The absence of effective compiler technology has resulted in lack of portability and low productivity in the programming of parallel machines. With these problems growing more serious, due to the popularization of parallelism and the complexity increase expected in future high-end machines, advances in compiler technology are now more important than ever. In this presentation, I will discuss the state of the long standing problem of automatic parallelization and describe new important lines of research such as the identification of levels of abstractions that help both productivity and compilation, the development of a solid understanding of the automatic optimization process, the creation of a research methodology to enable the quantification of progress, and the development of an effective methodology for the interaction of programmers with compilers.

10:00 AM – 12:00 PM Friday, December 18

Technical Session 4: Applications 1

On Accelerating Concurrent PCA Computations for Financial Risk Applications
Anubhav Jain, Mayank Bakshi, Amit Kalele and Easwar Subramanian (TCS Innovation Labs, Tata Consultancy Services, India)

A Performance Model for GPU-Accelerated FDTD Applications
Paul Baumeister and Thorsten Hater (Forschungszentrum Juelich, Germany); Jiri Kraus (NVIDIA, Germany); Dirk Pleiter (Forschungszentrum Jülich & Jülich Supercomputing Centre, Germany); Pierre Wahl (Vrije Universiteit Brussel and Luceda Photonics, Belgium)

Vectorized Big Integer Operations for Cryptosystems on Intel MIC Platform
Cheng Chang and Shun Yao (Stony Brook University, USA); Dantong Yu (BNL, Upton, USA)

Characterizing Large Dataset GPU Compute Workloads Targeting Systems with Die-Stacked Memory
Srividya Ramanathan, Gautam Hazari, Kanishka Lahiri, and Francesco Spadini (Advanced Micro Devices, Inc., India)

A GPU-based MIS Aggregation Strategy
T. Lewis, Shankar Sastry, Mike Kirby and Ross Whitaker (University of Utah, USA)

High Throughput Hierarchical Heavy Hitter Detection in Data Streams
Da Tong and Viktor K. Prasanna (University of Southern California, USA)

Industry BoF Sessions (see previous page for details)

INTEL @ 10:00 AM • SHELL @ 10:00 AM • AMD @ 1:00 PM • SanDisk @ 3:30 PM

1:00 PM – 3:00 PM Friday, December 18

Technical Session 5: High Performance Communication and Energy Efficient Computing

Offloaded GPU Collectives using CORE-Direct and CUDA Capabilities on IB Clusters
Akshay Venkatesh, Khaled Hamidouche, Hari Subramoni and Dhabaleswar Panda (The Ohio State University, USA)

High Performance OpenSHMEM Strided Communication Support with InfiniBand UMR
Mingzhe Li, Khaled Hamidouche, Xiaoyi Lu, Jie Zhang, Jian Lin and Dhabaleswar Panda (The Ohio State University, USA)

On the Use of Commodity Ethernet Technology in Exascale HPC Systems
Mariano Benito, Enrique Vallejo and Ramon Beivide (University of Cantabria, Spain)

Trigeneous Platforms for Energy Efficient Computing of HPC Applications
Santhosh Rethinagiri (BSC-Microsoft Research Centre & Barcelona Supercomputing Center, Spain); Oscar Palomar, Francisco Javier Arias Moreno, Adrian Cristal and Osman Unsal (Barcelona Supercomputing Center, Spain)

ColdBus: A Near-Optimal Power Efficient Optical Bus
Eldhose Peter, Arun Thomas, Anuj Dhawan and Smruti Sarangi (Indian Institute of Technology Delhi, India)

A Simple BSP-based Model to Predict Execution Time in GPU Applications
Marcos Amarís, Alfredo Goldman and Daniel Cordeiro (University of São Paulo, Brazil); Raphael de Camargo (Universidade Federal do ABC, Brazil)

3:30 PM – 5:30 PM Friday, December 18

Technical Session 6: Load Balancing and GPU Algorithms

Partition with side effects
Fanny Pascual (Universite Pierre et Marie Curie, Poland); Krzysztof Rzadca (University of Warsaw, Poland)

Geographically Distributed Load Balancing with (Almost) Arbitrary Load Functions
Piotr Skowron and Krzysztof Rzadca (University of Warsaw, Poland)

Memory-Efficient Parallelization of 3D Lattice Boltzmann Flow Solver on a GPU
Nhat-Phuong Tran and Myungho Lee (MyongJi University, Korea) ; Dong Hoon Choi (Korea Institute of Science and Technology Information, Korea)

Accelerating Complex Event Processing through GPUs
Prabodha Srimal Rodrigo and Herath Mudiyanselage Nelanga Dilum Bandara (University of Moratuwa, Sri Lanka); Srinath Perera (WSO2 Inc. & University of Moratuwa, Sri Lanka)

Efficient Batched Predecessor Search in Shared Memory on GPUs
Benjamin Karsin, Henri Casanova and Nodari Sitchinava (University of Hawai'i at Mānoa, USA)

Strategies of SIMD computing for image coding in GPU
Pablo Enfedaque, Francesc Auli-Llinas and Juan Carlos Moure (Universitat Autónoma de Barcelona, Spain)

Starting 7:00 PM Friday, December 18

- **Cultural Event: Hindustani Classical Music Concert, featuring Sri Sameer Rao**
- **Followed by HiPC 2015 Banquet (Special Dinner Buffet Menu at Park Plaza)**

Day 4 - Saturday, December 19

Breakfast @ 7:00, Break@ 9:30, Lunch @ 12:00

8:30 AM – 9:30 AM Saturday, December 19

HiPC 2015 Keynote Presentation 3:
The Architecture of Smart Phones

Speaker: Trevor Mudge
(Bredt Family Professor of Engineering, University of Michigan)

Abstract: The growth of the smart-phone market has been phenomenal. I don't need to quote exact numbers, which are in the hundreds of millions, to illustrate their ubiquity —- most of us have a smart-phone in our pocket. The design constraints on smart phones are among the most challenging in computing: 1) low power to preserve battery life; 2) base-band processors to support 4G data rates (100 Mbs — moving to 1Gbs for 5G); 3) multicore application processors for ever more sophisticated applications; and 4) time-to-market constraints that often result in solutions that seem ad hoc at best. Smart phones have become by far the most important of today's computing platforms. Oddly, the computer architecture community has been slow to recognize this. There are only an handful of published studies that attempt to provide an architectural perspective. This talk will review the current state of the architecture of mobile phone platforms, and present some initial studies that the author and his research group have conducted on existing systems. Suggestions for future research and future architectures will be presented.

10:00 AM – 12:00 PM Saturday, December 19

Academic Birds-of-a-Feather 1:
Advanced Numerical Schemes for Massively Parallel Computing: Challenges and Opportunities

Abstract: Many physical phenomena and industrial processes are described by a set of partial differential equations (PDEs), and almost all of these PDE models are coupled and nonlinear in nature. Most popular methods for solving PDEs are the finite difference method, finite volume method and finite element method. Applying one of these methods to model problems results in a large sparse system of (mostly linear) algebraic equations. In general, the size of the system will be few hundred millions, and solving these huge systems is impossible without supercomputers. Apart from other challenges associated with the parallel implementations, parallel computations require not only efficient parallel algorithms, but also highly scalable numerical methods. Moreover, the supercomputing architecture is moving toward massive parallelism with millions of cores and use of hardware accelerators. This requires a fundamental change in the methods, algorithms and implementations to exploit full compute power from these architectures. The development of robust and efficient high order algorithms and their use in HPC systems is an active research area. It is the purpose of this session to discuss the challenges and opportunities in developing parallel, efficient and scalable numerical schemes for massively parallel supercomputers. The topics to be discussed include: scalable and robust high order schemes; high performance numerical linear algebra; efficient implementations; scalable time integration strategies; and algorithms for GPUs, heterogeneous systems.

Organizers:

- Sashikumaar Ganesan, IISc, Bangalore
- Praveen C, TIFR-CAM, Bangalore
- Biswajit Mishra, Shell Technology Center, Bangalore

10:00 AM – 12:00 PM Saturday, December 19

Technical Session 7: Cloud and Data-Intensive Computing

IC-Data: Improving Compressed Data Processing in Hadoop
Adnan Haider, Xi Yang and Ning Liu (Illinois Institute of Technology, USA); Shuibing He (Computer School of Wuhan University, P.R. China); Xian-He Sun (Illinois Institute of Technology, USA)

Dominoes: Speculative Repair in Erasure Coded Hadoop System
Xi Yang (Illinois Institute of Technology, USA); Chen Feng (Institute of Computing Technology, P.R. China); Zhiwei Xu (Institute of Computing Technology, Chinese Academy of Sciences, P.R. China); Xian-He Sun (Illinois Institute of Technology, USA)

Collective Offload for Heterogeneous Clusters
Vicenç Beltran, Jesús Labarta and Florentino Sainz (Barcelona Supercomputing Center, Spain)

Meta-scheduling of HPC Jobs in Day-Ahead Electricity Markets
Prakash Murali and Sathish Vadhiyar (Indian Institute of Science, India)

Load Balancing and Accelerating Spatial Join Operations using Bitmap Indexing
Sameh Abdulah (The Ohio State University, USA); Yu Su (Facebook, USA); Gagan Agrawal (The Ohio State University, USA)

Algorithm Level Fault Tolerance for Molecular Dynamic Applications
Jiaqi Liu and Gagan Agrawal (The Ohio State University, USA)

1:30 PM – 3:30 PM Saturday, December 19

Technical Session 8: Applications 2

V-PFORDelta: Data Compression for Energy Efficient Computation of Time Series
Abdullah Al Hasib, Juan Cebrián and Lasse Natvig (Norwegian University of Science and Technology, Norway)

Holistic Management of Sustainable Geo-Distributed Data Centers
Zahra Abbasi (Ericsson Research, USA); Sandeep Gupta (Arizona State University, USA)

Parallel Megabase DNA Sequence Comparison with OpenCL
Marco Figueiredo, Jr., Edans Flavius de Oliveira Sandes, and Alba Cristina Magalhaes Alves de Melo (Universidade de Brasilia, Brazil);

Parallel Read Error Correction for Big Genomic Datasets
Nagakishore Jammula (Georgia Institute of Technology, USA); Sriram Chockalingam (Indian Institute of Technology, Bombay, India); Srinivas Aluru (Georgia Institute of Technology & Indian Institute of Technology Bombay, USA)

High Performance Front Camera ADAS Applications on TI's TDA3X Platform
Mihir N. Mody, Pramod Swami, Kedar Chitnis, Shyam Jagannathan, Kumar Desappan, Anshu Jain, and Deepak Poddar (Texas Instruments Pvt Ltd, India); Zoran Nikolic (Texas Instruments, USA); Prashanth Viswanath, Manu Mathew and Soyeb N Nagori (Texas Instruments Pvt Ltd, India); Hrushikesh Garud (Texas Instruments Pvt Ltd, Bangalore & School of Medical Science and Technology, IIT Kharagpur, India)

Information Theory Based Genome-scale Gene Networks Construction using MapReduce
Sriram Chockalingam (Indian Institute of Technology, Bombay, India); Maneesha Aluru (Georgia Institute of Technology, USA); Srinivas Aluru (Georgia Institute of Technology & Indian Institute of Technology Bombay, USA)

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